département instruments

3D-1-7231

ENERTEC

7600 LOGIC ANALYZER
PART: **USER GUIDE**

7600 LOGIC ANALYZER

ENERTEC
Schlumberger

ENERTEC
Schlumberger

ENERTEC
DÉPARTEMENT INSTRUMENTS
5, RUE DAGUERRE 42030 SAINT-ÉTIENNE
CEDEX FRANCE TÉL. (77) 25 22 64
TÉLEX 330696 CIRCE STETN
ADRESSE TÉLÉGRAPHIQUE CIRCE ST-ÉTIENNE

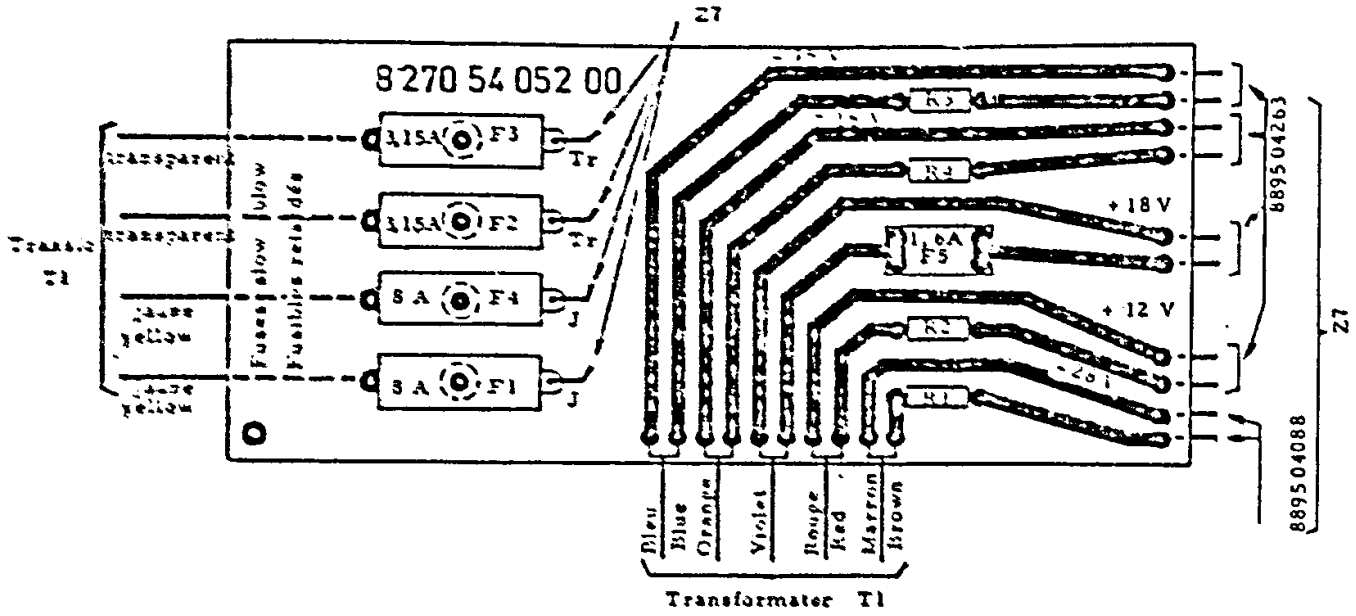
7600 LOGIC ANALYZER

-:-:-:-:-:-:-:-:-:-:-:-:-:-:-:-

Valable pour commande
-750008-

76020 OPTION

- The 115 V position is added on the mains selector S1.
- Z16 printed circuit board with 5 fuses is added on the secondary part of transformer T1 as follows:



Fuses :

F1 : 8 A
F2 : 3.15 A
F3 : 3.15 A
F4 : 8 A
F5 : 1.6 A

Resistors :

R1 : 47 Ω
R2 : 0.22 Ω
R3 : 1 Ω
R4 : 0.68 Ω

800603

TABLE OF CONTENTS

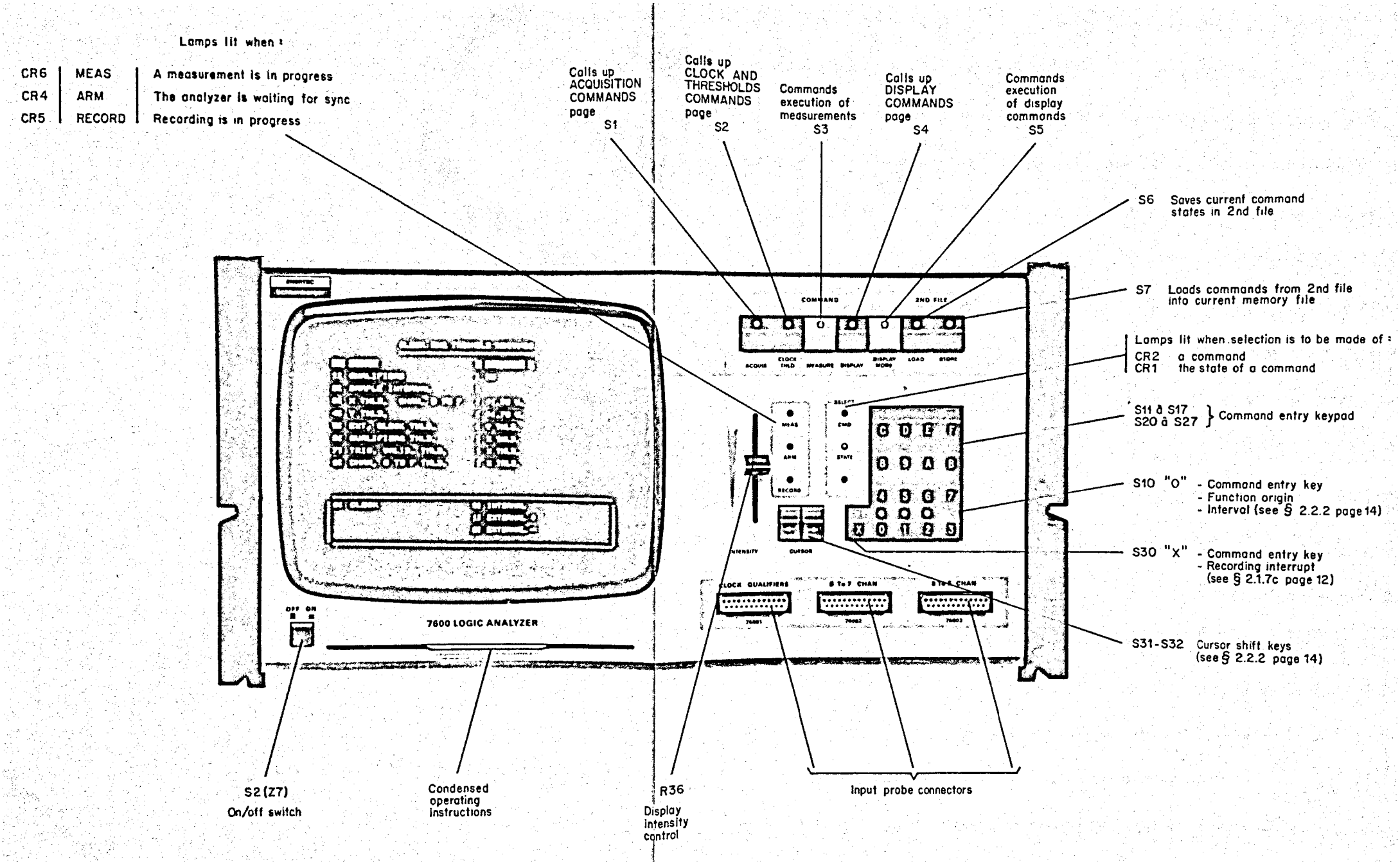
	PLATE
P1	Front view
P2	Rear view
P3a	Top view
P3b	Left side view
P4	Z1
P5	Z2
P6	Z3
P7	Z4
P8	Z6
P9	Z7 - Z8 - Z10
P10	Data display

PAGES	1. - TECHNICAL SPECIFICATIONS
1	1.1 . - General
2	1.2 . - Memory capacity
	1.3 . - Characteristics common to all inputs
3	1.4 . - Clock
	1.4.1. - Internal clock period
	1.4.2. - External clock
	1.4.3. - External clock qualifier inputs CQØ and CQ1
4	1.5 . - Channels 0 to F and trigger qualifiers TQ0 to TQ3 inputs
	1.6 . - External stepping rate input
	1.7 . - Sync output
5	1.8 . - Operating environment
	1.9 . - Power requirements
	1.10. - Dimensions - Mass
	1.11. - Accessories
	2. - OPERATION
7	2.1 . - Data acquisition
	2.1.1. - Clock
8	2.1.2. - Logic threshold
	2.1.3. - Format selection - Truth table
9	2.1.4. - Stepping mode
10	2.1.5. - Triggering
11	2.1.6. - Offset
	2.1.7. - Recording mode

PAGES	
12	2. 1. 8. - Glitch detection
13	2.2 . - Data display
	2. 2. 1. - Acquisition mode recall
	2. 2. 2. - Levels diagram
15	2. 2. 3. - States diagram
	2. 2. 4. - Graph diagram
17	2. 2. 5. - Map diagram
18	2.3 . - Operating instructions
	2. 3. 1. - Command management
19	2. 3. 2. - Measurement
	2. 3. 3. - Display mode command
20	2. 3. 4. - Initial condition - command state storage
	2. 3. 5. - 2nd file
	2. 3. 6. - Automatic offset command
21	2.4 . - Command page lists.
	3. - CIRCUIT DESCRIPTION
26	3.1 . - General principles
28	3.2 . - Input probes
	3.3 . - Amplifier board Z1
31	3.4 . - Memory board Z2
34	3.5 . - Logic board Z31
	3. 5. 1. - Microprocessor
35	3. 5. 2. - Memories
36	3. 5. 3. - PIA s
37	3. 5. 4. - Interconnections between microprocessor, memories and PIA s
38	3. 5. 5. - X and Y thresholds
	3.6 . - Keyboard Z5
39	3.7 . - Display board Z4
43	3.8 . - CRT drive board
45	3.9 . - Power supply
	4. - MAINTENANCE
47	4.1 . - Front panel upkeep
	4.2 . - Equipment required for fault finding and setting up
	4.3 . - Access to printed circuit boards
48	4.4 . - Fault finding
49	4.5 . - Testing and setting up
	4. 5. 1. - Power supplies
	4. 5. 2. - Logic boards Z31 and Z4
50	4. 5. 3. - Sensitivity of the 23 input channels
	4. 5. 4. - Internal clocks
	4. 5. 5. - X and Y gains
51	4. 5. 6. - Trigger word
	4. 5. 7. - Trigger offset

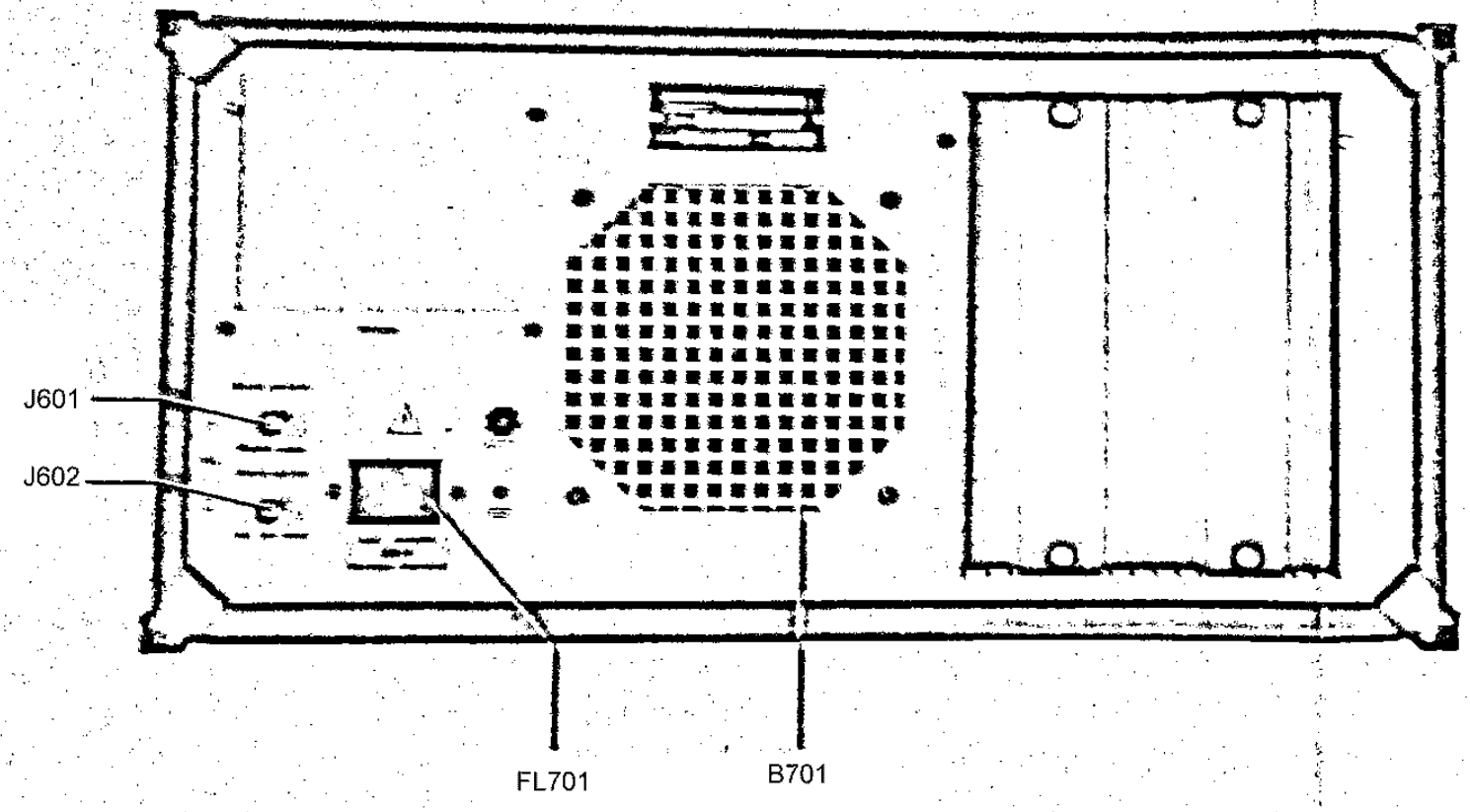
PAGES		
52		4. 5. 8. - Trigger qualifier channels
		4. 5. 9. - Measurement rate
		4. 5. 10. - External clock qualifier channels CQ0 and CQ1
53		4. 5. 11. - Glitch detect function on channels ∅ to 3
		4. 5. 12. - Threshold allocation
54		4. 5. 13. - Truth table
		4. 5. 14. - CRT drive circuit setting up
FIG.	5. - SCHEMATICS	
1		Amplifier
2		Memory
3		Logic
4		Display
5		Keyboard
6		Mother board
7		Power supply
8		CRT Drive
9		76001 probe
10		76002-3 probes
	6. - PARTS LIST	

7 xxxx 0002	Référence Fabricant des éléments repérés "N0" dans la nomenclature.
7 7600 0200	Panneau arrière
7 7600 0600/1 et 2	Assemblage mécanique - Habillage
7 7600 0800	Panneau avant
7 7600 1000	Sondes 76001, 76002, 76003
7 7600 1011/1 à 12	Carte amplificateur Z1 - fig. 1
7 7600 1021/1 à 5	Carte mémoire Z2 - fig. 2
7 7600 1311/1 à 4	Carte logique Z31 - fig. 3
7 7600 1041/1 à 4	Carte visualisation Z4 - fig. 4
7 7600 1051/1 et 2	Carte clavier Z5 - fig. 5
7 7600 1061	Carte plancher Z6 - fig. 6
7 7600 1071/1 et 2	Carte alimentation plancher Z7 - fig. 7
7 7600 1072	Carte alimentation arrière Z8 - fig. 7
7 7600 1073	Carte régulateurs Z10 - fig. 7
7 7600 1081/1 à 3	Carte commande tube - fig. 8
7 0094 1091/1 à 3	Carte entrée sonde Z9 - fig. 9
9 7600 6000	Pochette cordon 76006


Lamps lit when :
CR6 | MEAS | A measurement is in progress
CR4 | ARM | The analyzer is waiting for sync
CR5 | RECORD | Recording is in progress
Calls up ACQUISITION COMMANDS page
S1
Calls up CLOCK AND THRESHOLDS COMMANDS page
S2
Commands execution of measurements
S3
Calls up DISPLAY COMMANDS page
S4
Commands execution of display commands
S5
S6 Saves current command states in 2nd file
S7 Loads commands from 2nd file into current memory file
Lamps lit when selection is to be made of :
CR2 a command
CR1 the state of a command
S11 à S17
S20 à S27
Command entry keypad
S10 "0" - Command entry key
- Function origin
- Interval (see § 2.2.2 page 14)
S30 "X" - Command entry key
- Recording interrupt
(see § 2.1.7c page 12)
S31-S32 Cursor shift keys
(see § 2.2.2 page 14)
7600 LOGIC ANALYZER
S2 (Z7)
On/off switch
Condensed operating instructions
R36
Display intensity control
Input probe connectors

P2 VUE ARRIERE

REAR VIEW



12-03-80 HIVERT	7600	ENERTEC Schlumberger

1.- TECHNICAL SPECIFICATIONS

1.1.- GENERAL

The 7600 logic analyzer is capable of measurements on complex hardware and software systems, such as microprocessors, computers, peripherals, etc.

It can store 4096 data bits in the form of 256 16-bit words, 512 8-bit words or 1024 4-bit words, and also 4096 reference bits for the truth-table comparison function.

Commands and results are displayed directly on the integral 23 cm screen. A hexadecimal keypad with indicator lamps is used for command entry and dialogue with the user.

An auxiliary internal memory can store two complete files of commands, even during power interruptions.

Recording of data into memory is commanded by a trigger word, this word being qualified by four further inputs.

Triggering may be on true, when data configuration is identical to the qualified trigger word, or on FALSE, any configuration different from the qualified trigger word.

Data are processed at the rate set by an internal clock (100 MHz max.), or by an external clock (that of the system under test for example) ; synchronous and asynchronous operation are thus both possible.

Recording into memory is synchronized by a signal that can be offset with respect to the trigger signal by any number of clock periods from 0 to 65535. This sync signal is available on the rear panel. Recording may take place before or after this signal.

Data may be displayed in any of four modes :

- on a timing diagram showing levels (with normal, mixed or expanded scale) ;
- as states grouped in binary, hexadecimal, octal or ASCII words ; the recorded list can then be compared with the stored truth table ;
- in the form of a graph representing the binary values of the recorded words against time ;
- as a map diagram : each word is represented as a bright dot, of which the position on the X-axis is proportional to the least significant bits and the position on the Y-axis proportional to the most significant bits.

1.2. - MEMORY CAPACITY

Main memory : 4096 bits, in the form :

256 words of 16 bits (16-channel input)
512 words of 8 bits (8 - channel input)
1024 words of 4 bits (4 - channel input)

Truth table memory : 4096 bits.

1.3. - CHARACTERISTICS COMMON TO ALL INPUTS

- Signal frequency : 0 to 30 MHz
- Sensitivity : 400 mV peak to peak from 0 to 10 MHz
  800 mV peak to peak to 30 MHz
- Input impedance seen at probe pod tip :
  about 100 kΩ paralleled by about 7 pF (add about 4 pF with grip tips)
- Logic threshold at centre of hysteresis zone (sensitivity) :
  adjustable from + 6,35 V to - 6,35 V in 50 mV steps.
  Logic threshold accuracy : ± 50 mV ± 5 %.
- Maximum permissible input voltage : 100 V peak.

1.4. - CLOCK

The clock defines the rate at which input signals are sampled.

1.4.1. - Internal clock period

50 ns to 500 ms in 1 - 2 - 5 sequence for 16-bit words

20 ns to 500 ms in 1 - 2 - 5 sequence for 8-bit words

10 ns to 500 ms in 1 - 2 - 5 sequence for 4-bit words

Accuracy : $\pm$ 0.1 %.

1.4.2. - External clock

- Input on pin C of 76001 pod (see paragraph 1.3)
- Recording on rising or falling slope of signal
- Range : 0 to 30 MHz (typically 50 MHz ; 25 MHz in 16-channel format)
- Sensitivity - Input impedance - Logic threshold - Max. voltage : see paragraph 1.3
- Minimum time for data to be stable before slope of external clock signal : $\leq$ 20 ns
- Minimum time for data to be held after slope of external clock signal : $\leq$ 1 ns.

1.4.3. - External clock qualifier inputs, CQ$\emptyset$ and CQ1

- Inputs on the two pins CQ$\emptyset$ and CQ1 of 76001 pod. State 0, 1 or X (don't care) selectable for each channel : slope of external clock is qualified for acquisition of input channel data if the state of each clock qualifier channel corresponds to the selected state. Slope of external clock is ignored if one of the clock qualifiers is not satisfied.
- Range - Sensitivity - Impedance - Logic threshold - Max. voltage : see paragraph 1.3.
- CQ$\emptyset$ and CQ1 states : minimum time for :
  - stability before selected clock slope : $\leq$ 20 ns
  - hold after selected clock slope : $\leq$ 1 ns.

1.5. - CHANNELS 0 TO F AND TRIGGER QUALIFIERS TQ0 TO TQ3 INPUTS

Channels TQ0 to TQ3 on probe pod 76001.

Channels 0 to 7 on probe pod 76002.

Channels 8 to F on probe pod 76003.

- Channels 0 to F receive data signals to be recorded for analysis. in 8-bit and 4-bit formats, available non-recorded channels are used for trigger qualifying.
- For channels TQ0 to TQ3, which are not recordable, the operator defines the conditions (state 0, 1 or X) for qualifying the trigger word applied to the recorded channels.
- Frequency range - Sensitivity - Input impedance - Logic threshold - Max. permissible voltage : see paragraph 1.3.
- Dispersion of propagation time between channels : 5 ns.
- Smallest detectable pulse width :

  15 ns with about 800 mV peak to peak
  10 ns with about 3 V peak to peak.

1.6. - EXTERNAL STEPPING RATE INPUT (rear panel)

- When external stepping is selected, this input receives a negative pulse which :
  - . initializes the analyser when low
  - . enables data acquisition on returning to high.
- Pulse : . TTL levels
  - . quiescent level : high
  - . minimum width : 50 ns
- Fan-in : 1 TTL-LS input and 1 10-kΩ resistor to + 5 V.

1.7. - SYNC OUTPUT

- Transition from high to low (TTL levels) is synchronized with start or end of recording, depending on selected mode.
- Transition corresponds to qualified trigger word, offset by N clock periods when analyzer has been initialized for a measurement. (N = 0 to 65535).

1.8. - OPERATING ENVIRONMENT

- Operating temperature range : 0° to + 50°C
- Performance guaranteed : + 10° to + 40°C
- Storage temperature range : - 20° to + 65°C.

1.9. - POWER REQUIREMENTS

Mains voltage : 110 - 127 - 220 - 240 V rms, ± 10%

Mains frequency : 50 or 400 Hz

Power consumption : about 245 VA

Fuses : 110 - 127 V : 3.15 A
220 - 240 V : 1.6 A

Safety requirements conform to IEC 348 class I apparatus.

1.10. - DIMENSIONS - MASS

Dimensions : height : 230 mm
width : 445 mm
depth : 485 mm

Mass : 17.8 kg

1.11. - ACCESSORIES

Supplied with instrument

- 1 technical manual
- 1 mains lead, P/N 8315 000 29
- Three probe pods : clock and qualifier inputs P/N 7x001
channels 0 to 7 inputs, P/N 7x002
channels 8 to F inputs, P/N 7x003
- Set of 30 leads with 2-mm male pins and grip tips, P/N 7x000

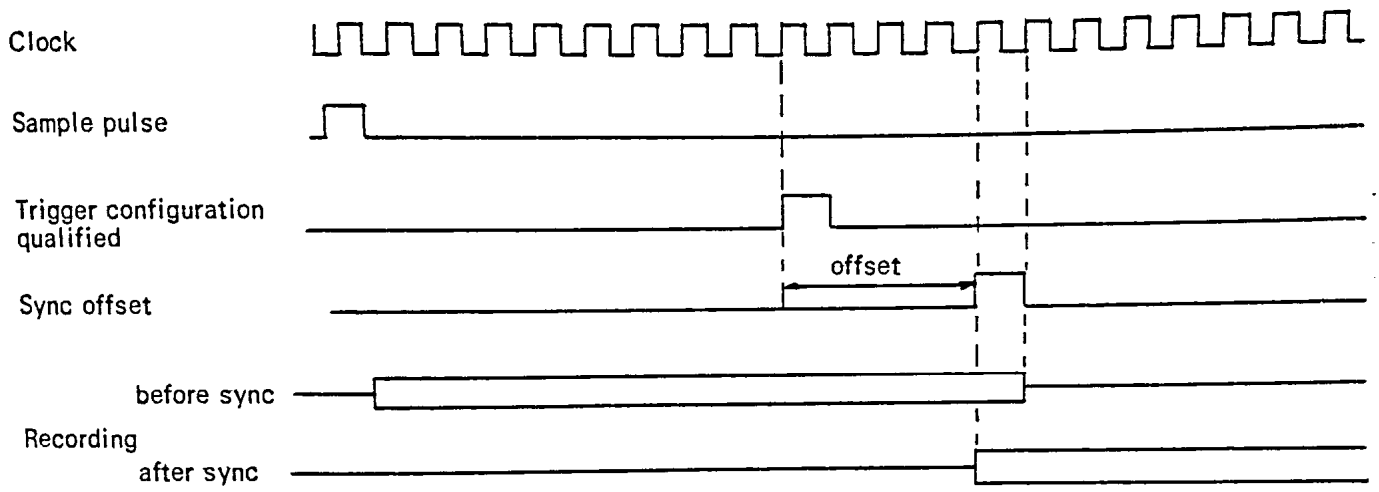
Optional accessories

P/N :	
76001	Clock and qualifier inputs probe pod
76002	Channels 0 to 7 inputs
76003	Channels 8 to F inputs
76004	RS232 and IEC GP-IB 1/0 and programming card
76005	Rack mounting kit (5U)
76006	Set of 30 leads with 2-mm male pins and grip tips
76007	Set of 30 leads with 2-mm male pins and wire-wrap tips
76008	Three 10-wire adaptor blocks for 76001, 76002 and 76003 probe pods
76009	Three extender cables for connecting probe pods to 7600. Length : 1.50 m.
76010	Three hook clips for probe pods
7601	Extension to 32 channels

2. - OPERATION

2.1. - DATA ACQUISITION

The timing diagram that follows shows the timing of the various data acquisition signals.



2.1.1. - Clock

The logic signals at the input are sampled at the rate set by a clock. Depending on whether internal or external clock is selected, operation of the logic analyzer is synchronous or asynchronous.

a) Asynchronous operation

The internal clock used has no phase relationship with the input signals.

The user can select the rate (in steps in 1 - 2 - 5 sequence), in the ranges : 50 ns to 500 ms in 16-channel format
20 ns to 500 ms in 8-channel format
10 ns to 500 ms in 4-channel format.

b) Synchronous operation

The external clock (in general the clock of the system under test) is connected to the C input of the 76001 probe pod.

Sampling can take place on the rising ⎍ or the falling ⎎ slope of the clock. Qualification of the selected slope can be controlled via the CQØ and CQ1 inputs of the 76001 pod by state Ø, 1 or X (don't care).

Only those clock slopes that arrive when inputs CQØ and CQ1 are in the states defined by the user are qualified for data sampling. This feature enables data that are useful for system analysis to be selected out of a stream.

2.1.2. - Logic threshold

The logic analyzer only recognizes input signals as carriers of binary information. The input signal is only retained as a level with respect to a threshold :

- high if the input voltage is above the threshold
- low if the input voltage is below the threshold.

Depending on the logic convention in use :

positive logic is : high level = 1 state
low level = Ø state

negative logic is : high level = Ø state
low level = 1 state.

The 7600 logic analyzer can operate with 2 different logic thresholds depending on the inputs, called threshold X and threshold Y. The values of these thresholds are selected in the range - 6.35 V to + 6.35 V in 50 mV steps.

The user can then assign one or other of these thresholds to the following groups of input channels : 8 to F (76003), external clock, external clock qualifiers, trigger qualifiers. Threshold X is arbitrarily assigned to channel group 0 to 7 (76002 pod).

2.1.3. - Format selection - Truth table

In order to make best use of the 4096-bit memory capacity, the user can select one of 3 data formats using 4, 8 or 16 channels :

- 16 channels for recording 256 words of 16 bits
- 8 channels for recording 512 words of 8 bits
- 4 channels for recording 1024 words of 4 bits.

The maximum sample rate depends on the format selected :

Format	Channels stored	SAMPLE RATE with internal clock	with external clock
16 channels	0 to F	20 MHz (50 ns)	25 MHz (40 ns)
8 channels	0 to 7	50 MHz (20 ns)	30 MHz (33 ns) 50 MHz (20 ns) *
4 channels	0 to 3	100 MHz (10 ns)	30 MHz (33 ns) 50 MHz (20 ns) *

* typical value

Truth table

The auxiliary memory of 4096 bits, called Truth Table, is intended for reference data. In COMPARE mode its contents are compared with those of the Data memory (see paragraph 2.2.3).

This table is also used in the HALT IF DIFFERENT sample mode.

Transfer of memory contents can be executed in 3 ways :

- transfer of Data memory contents to Truth Table memory (Data memory contents remain unchanged)
- transfer of Truth Table memory contents into Data memory (Truth Table contents unchanged)
- exchange of contents between Data and Truth Table memories.

The user can thus employ all the display modes for analyzing the Truth Table contents.

2.1.4. - Stepping mode

To make a measurement, the logic analyzer must be armed or initialized in one of the following ways :

- Automatic stepping : the analyzer rearms itself after each measurement with a wait time selected from 0 - 0.3 - 1 and 10 seconds.
- External stepping : the analyzer is armed by a signal applied to the EXT STEP input on the rear panel. A stepping pulse applied during the acquisition phase re-initializes the analyser.

- Manual stepping : the analyzer is armed by pressing the MEASURE key on the front panel.
- HALT IF DIFFERENT stepping : the analyzer records in memory the data at its inputs and compares them with the Truth Table contents :
    - if the two are identical it rearms itself in order to execute a fresh record operation ;
    - if the two are different (only one bit different is enough) it displays on the screen the data that have just been recorded, in the selected display mode.

HALT IF DIFFERENT stepping should be used with care with BEFORE TRIGGER recording and in 8 and 4-channel formats, since in this stepping mode the start of recording depends on the sample rate. In addition, in 8 (4) channel format there may be a 1 (3) clock period offset in data recording, since recording is executed by blocks of 16 bits (see next paragraph).

2.1.5. - Triggering

The start or end of recording depends on detection of the trigger word in the stream of input data on the 16 recordable channels. This word is qualified by means of 4 additional inputs, which are not recordable.

The unused input channels in 8-bit and 4-bit formats can also be used for qualifying the trigger word.

Triggering thus occurs on 20 bits : either 16 + 4 bits (16-channel format) or 8 + 8 + 4 bits (8-channel format) or 4 + 12 + 4 bits (4-channel format).

For each channel the user can select one of the states 0, 1 or X (don't care). Once the trigger configuration has been defined he can then choose between two modes :

a) True trigger : triggering occurs when the analyzer finds, on the recordable and qualifier channel inputs (sampled by the clock), a configuration identical to that selected.

b) False trigger : triggering occurs when the analyzer finds, on the sampled inputs, a configuration different from that selected.

The result of comparison of the input configuration (recordable channels and trigger qualifier channels) with the programmed trigger word is given with a delay of about 15 ns.

2.1.6. - Offset

Recording into memory is synchronized, starting from the trigger word, word, after a delay of N clock pulses where N may take any value from 0 to 65 535.

By using this offset, the zone of data recorded can be moved about in the input data stream without changing the trigger commands.

The sync signal (delayed trigger) is provided on the ⅂ SYNC OUTPUT coaxial connector on the rear panel (see paragraph 1.7).

Offset can be calculated by the analyzer, using AUTO OFFSET function. The user only needs to indicate the start or stop point of recording for the following acquisition cycles in the data stream (see paragraph 2.3.6).

2.1.7. - Recording mode

Data on inputs of recordable channels can be recorded before or after sync.

a) Recording before sync.

- the analyzer starts storing recordable input data as soon as it is armed
- the sync signal stops the recording process
- if the data exceed memory capacity, the analyzer only retains the most recent data, corresponding to total capacity of the Data memory.

The Data memory is organized in 256 words of 16 bits. When 8-bit format is selected, the analyzer records two 8-bit words simultaneously ; in 4-bit format, it records four 4-bit words simultaneously. In both these cases the data word corresponding to sync (trigger word + delay) forms part of the last group of words recorded. If several consecutive measurements are made in before-sync recording mode, there may thus be a jitter of 2 words (in 8-bit format) or of 4 words (in 4-bit format), as seen on the screen.

b) Recording after sync

In this recording mode the sync signal gives the command to start recording, which normally ends when the Data memory is full.

c) Recording interruption

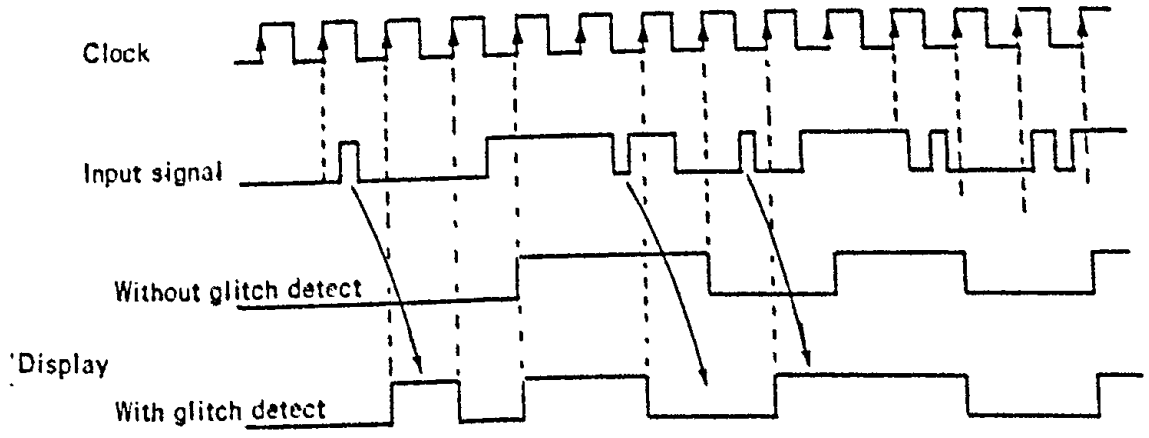
If measurement should become stuck during recording for any reason (for example because of failure of the clock of the system under test, in synchronous operation), the user can interrupt recording by pressing the [N] key on the front panel keypad. The analyzer will then yield the partial result of the measurement.

2.1.8. - Glitch detection

Since the input signals are sampled at a rate set by a clock, it can often be useful to investigate input states between two clock edges, in particular with slow clock rates.

For this purpose the four recordable inputs 0, 1, 2 and 3 have a switchable GLITCH DETECT feature. This feature detects any glitch spikes between two clock edges, and warns the user by changing the state of the input signal on the next clock period (see diagram below).

The GLITCH DETECT feature is only provided on channels 0 to 3, but the user can connect two inputs in parallel, one with glitch detect, the other without. On comparison of the signals recorded by these channels, the points where glitch spikes have been detected immediately become obvious.



GLITCH DETECT can not be selected with the internal 100 MHz clock ; but in this mode the clock signal is in any case faster than the shortest detectable spike.

2.2. - DATA DISPLAY

Recorded data can be displayed in any of four different ways : timing states, graph or map diagrams.

2.2.1. - Acquisition mode recall

In the top right-hand corner of the screen the analyzer shows :

- the configuration of 20 bits selected for triggering
- the offset between trigger and sync
- clock in use
- use of GLITCH DETECT if selected.

The analyzer also shows whether the displayed results come from the Truth Table. This indication is particularly useful when the user is examining recorded and Truth Table data in turn, using the DATA ⇄ TABLE EXCHANGE command.

During the first measurement (after the MEASURE key is pressed) the analyzer shows progress with the measurement, by displaying the messages AWAITING SYNC and RECORDING on the screen.

During the recording phase the [N] key on the keypad is active, and can be used for interrupting recording.

2.2.2. - Timing diagram

In this display mode the analyzer displays the sequence of high and low levels for each channel recorded :

- each page contains 252 words ;
- channel numbers are displayed on the screen, to the left of the data from each channel.

Channels displayed :

A command is provided to enable the user to select the number of channels displayed on the screen. If the number selected is 8 or less the analyzer automatically expands the vertical scale of the display.

Display cursor

In the set of words recorded, each word is identified by a number in the sequence form 0 to 255 in 16-channel format, from 0 to 511 in 8-channel format, and from 0 to 1023 in 4-channel format. The display cursor can be used for marking any particular word with a bright vertical line. This line is shifted by pressing the ⟵ and ⟶ keys. The last line on the screen shows the number of the page being displayed, the number in the sequence of the word marked by the cursor, and the binary value of this word.

Interval function

The interval is the spacing of two words identified by the cursor, expressed in number of qualified clock periods :

- the first word is designated as origin of the interval measurement by pressing the [0] key when the cursor is on this word ;
- the interval between cursor position and this origin is displayed on the last line of the screen, after page number and cursor information. It is expressed in number of qualified clock periods.

Scale command

A scale command is provided for expanding the horizontal scale of the display :

- normal scale : 252 words per page. The first word on the left corresponds to positions 0 - 252 - 504 - 756 or 1008 in memory. The page displayed is that which contains the display cursor.
- expanded scale : 25 words per page (x 10 expansion). The word marked by the display cursor is located on the left-hand edge of the screen.
- mixed scale : this is a compromise between the two modes just described. Display is with normal scale from the origin of the page (0, 252, 504, 756 or 1008) up to the display cursor, after which it is with expanded scale. This mode is used for expanding a zone of the recorded data while keeping this zone within the general context of the recorded data.

2.2.3. - States diagram

In this display mode the analyzer displays the sequence of logical states corresponding to the recorded data. According to whether the user has selected positive or negative logic, the analyzer assigns logic state 1 or Ø to high level.

Code :

The recordable input channels are separated into two groups : channels 0 to 7 and channels 8 to F. For each group the user can select data display in binary, octal, hexadecimal or ASCII code.

In ASCII only the alphanumeric characters 0 to 9 and A to Z are recognized ; the signal from the channel with the highest weighting (the parity bit) is displayed in binary. When a word does not correspond to an alphanumeric character in ASCII, it is displayed in binary.

The analyzer displays :

- the sequence number of the word marked by the cursor with, opposite this word :
- the sequence numbers and states of the next 15 words.

By shifting the cursor the user can thus run through all the recorded data.

Comparison function

The analyzer displays the recorded data and the reference data in the truth table, in the selected code.

The differences between the two appear in inverted video (black on white background) in the list of displayed data.

2.2.4. - Graph diagram

On the graph diagram display data are shown in the form of a curve, with the recording sequence (i.e. time) as the X-axis and the binary value of the recorded word as the Y-axis ; the channel 0 bit is taken as least significant weighting.

The X-axis can display 126 words per page. The origin corresponds to cursor positions 0 - 126 - 252 - 378 - 504 - 630 - 756 - 882 - 1008. The page displayed is the one containing the cursor. The cursor can be shifted by the user ; its location is shown by intensification of the marked dot.

The vertical axis has resolution of 128 levels (7 bits). It has 16 graduations, from 0 to F. Two extra lines, at the top (marked -) and at the bottom (marked -), correspond to words that overflow upwards and downwards.

Selection of graph domain

To define the vertical scale, the user must :

- select the channel with the highest significant weighting to be accommodated on the graph, and
- select states for the channels of more significant weighting than the channel previously selected.

Example

In 16-channel format, if the user selects channel B as highest significant weighting, he must define the graph domain by assigning states (0 or 1) to channels C to F, which are more significant than B.

For example : F E D C
1 0 1 0

Since resolution is 7 bits, only channels B, A, 9, 8, 7, 6 and 5 will be shown on the graph.

The graph will therefore lie between :

	F E D C	B A 9 8 7 6 5	4 3 2 1 0
. minimum value :	1 0 1 0	0 0 0 0 0 0 0	X X X X X
. maximum value :	1 0 1 0	1 1 1 1 1 1 1	Y Y Y Y Y
	highly weighted bits, that define graph domain.	7 bits of graph	less significant bits, that do not contribute to the graph.

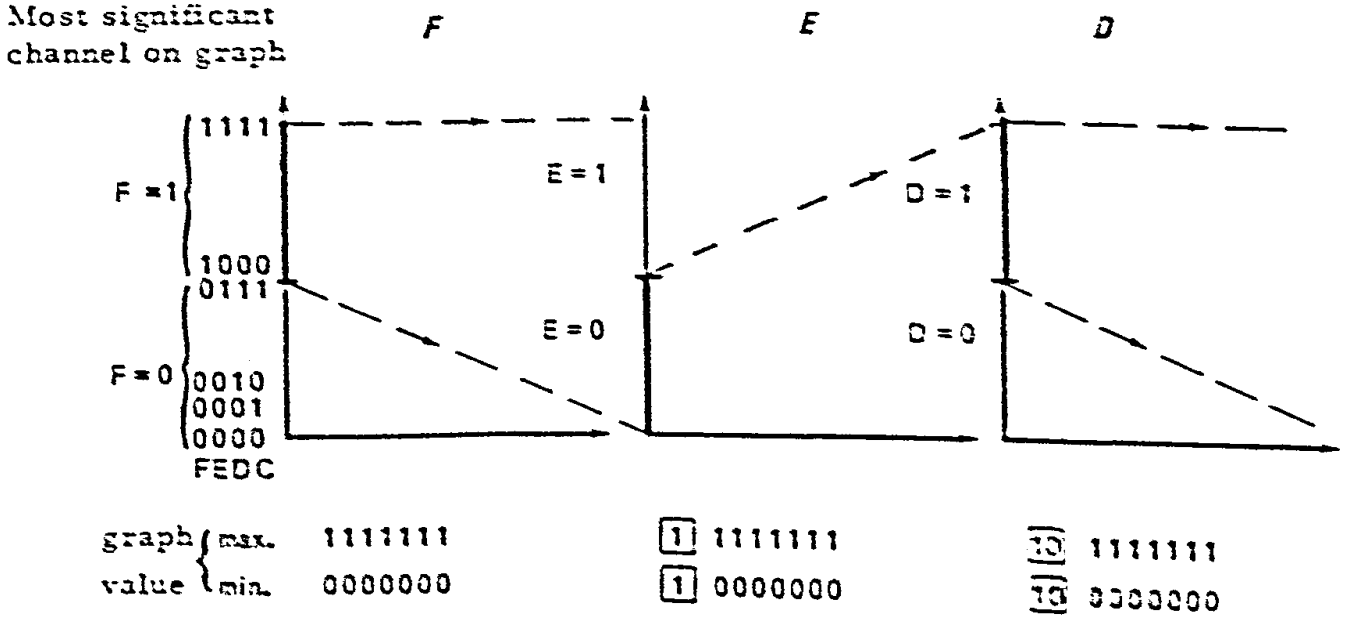
Example of graph diagram

[ ] : channels with weighting higher than that of the most significant channel on the graph : their states define the domain of the graph.

. : 7 bits shown on the graph.

X : bits that do not contribute.

Most significant channel on graph	F E D C B A 9 8 7 6 5 4 3 2 1 0
F	. . . . X X X X X X X X X
E	[1] . . . . X X X X X X X X
D	[1 0] . . . . X X X X X X X X
C	[1 0 1] . . . . X X X X X X X
B	[1 0 1 1] . . . . X X X X X X
A	[1 0 1 1 0] . . . . X X X X X
9	
'	
'	
'	
6	[1 0 1 1 0 1 1 1 0] . . . .



Interval function : see page 14.

2.2.5. - Map diagram

This is also a graphic representation of data recorded during the acquisition phase, with the value of the less significant weighting on the horizontal axis and the value of the more significant weightings on the vertical axis.

- 16-channel format : channels 0 to 7 are on the horizontal axis, and channels 8 to F on the vertical axis.
- 8-channel format : channels 0 to 3 are on the horizontal axis, and channels 4 to 7 are on the vertical axis.
- 4-channel format : channels 0 and 1 are on the horizontal axis, and channels 2 and 3 are on the vertical axis.

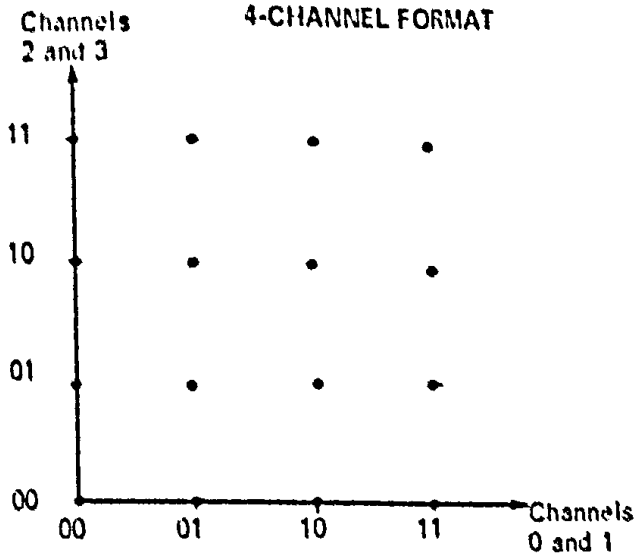
Each word recorded is thus shown as a dot on the map of all possible states.

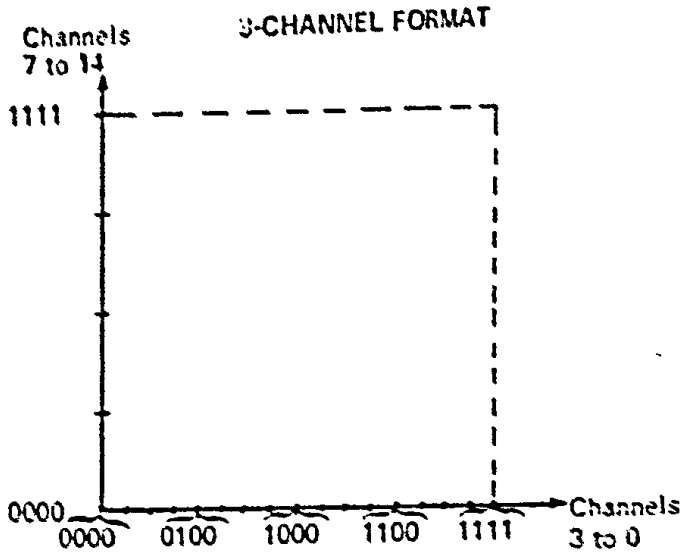
The word marked by the display cursor is shown up by intensification.

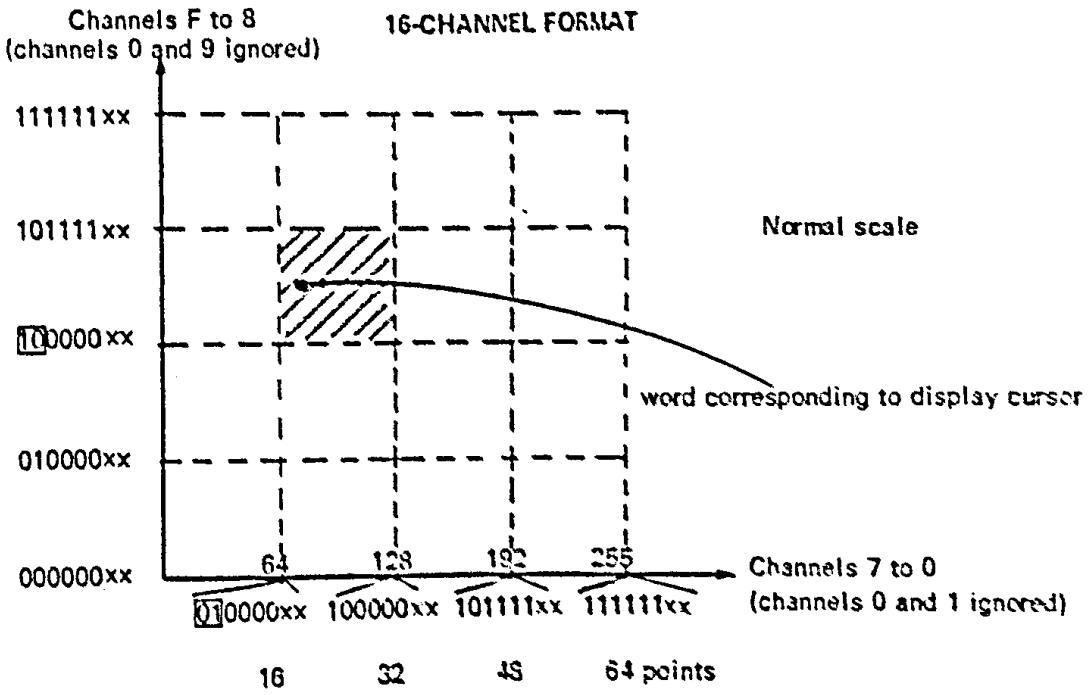
The "cloud" of dots shown on the screen gives the user a qualitative view of what has been recorded, at a single glance. A data dot that lies outside the zone expected by the user is thus immediately shown up.

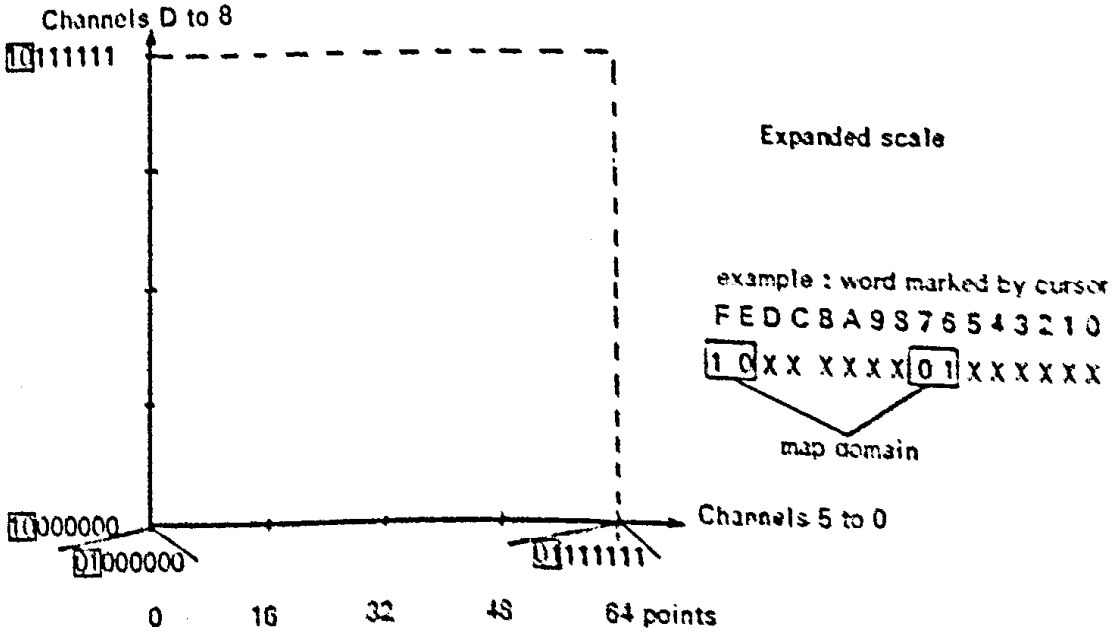
Normal scale

- In 4-channel format : there are 4 possible values for each axis, giving 16 possible values on the diagram.
- In 8-channel format : there are 16 possible values for each axis, giving 256 possible values on the diagram.
- In 16-channel format : there are 256 possible values for each axis. Since display resolution is only 64 points per axis (i.e. 6 bits), the two least significant channels on each axis are ignored; these are channels 0 and 1 on the horizontal axis and 8 and 9 on the vertical axis. To gain access to these channels the user can call up expanded scale (which is only available in 16-channel format), giving expansion by a factor of 16 of the area marked by the cursor.


Channels 2 and 3
4-CHANNEL FORMAT
11
10
01
00
00
01
10
11
Channels 0 and 1


Channels 7 to 14
1111
0000
0000
0100
1000
1100
1111
Channels 3 to 0


Channels F to 8
(channels 0 and 9 ignored)
16-CHANNEL FORMAT
111111xx
101111xx
100000xx
010000xx
000000xx
64
128
192
255
Normal scale
word corresponding to display cursor
Channels 7 to 0
(channels 0 and 1 ignored)
010000xx
100000xx
101111xx
111111xx
16
32
48
64 points


Channels D to 8
111111
Expanded scale
example : word marked by cursor
FEDCBA9876543210
10XX XXXX01XXXXXX
map domain
100000
010000
000000
111111
Channels 5 to 0
0
16
32
48
64 points

Expanded scale

In this case a map of 64 by 64 points is displayed as with normal scale, but the 6 least significant channels of each axis are taken into account (these are 0 to 5 on the horizontal axis and 8 to D on the vertical axis). On this map all data words that have the same values for the most significant channels (6, 7 and E, F respectively) are displayed.

A small map, on the left of the screen, shows where the expanded zone lies on the normal-scale map.

Interval function : see page 14.

2.3. - OPERATING INSTRUCTIONS

2.3.1. - Command management

The commands for the logic analyzer are listed on three pages that can be displayed on the screen. They cover, respectively :

. acquisition commands (see page 22)

. clock and threshold commands (see page 23)

. display commands (see pages 24 and 25).

- The user can call up any page by pressing the corresponding black key in the COMMAND group : ACQUIS CLOCK THLD and DISPLAY. The analyzer then will display the list of commands on that page, assigning each one a number, and also the state of each command at that moment.
- The SELECT CMD lamp will light to indicate that a command must be selected. The keyboard keys corresponding to the list of available commands will also light. Now depress the key with the number of the selected command.
- This command will now be displayed in inverse video (black on white) for emphasis.
- The various states possible for the selected command will be displayed in a box at the bottom of the screen, along with the corresponding numbers and instructions, if needed, for changing the command state.

- The SELECT STATE lamp will also light, along with the keys corresponding to possible states. Press one of these keys.
- If the command state is now fully defined, the analyzer will now return to the initial phase and list the commands on the page with their new states.
- If several keyboard operations are needed for full definition of a command state, the analyzer remains in the second phase (selection of state of a previously chosen command). When the command is fully defined, return to the COMMAND group keys to call up either another command on the same page, or else another page.

2.3.2. - Measurement execution command

When the commands on the three pages are in the required states, press the orange MEASURE key in the COMMAND group.

The MEAS lamp will light. The ARM and RECORD lamps show the user which phase of acquisition is in progress : analyzer armed and waiting for sync, or recording phase.

During recording, the [X] key lights. Pressing this key stops the recording phase (see paragraph 2.1.7.c).

After recording , the results are displayed on the screen in the selected display mode.

2.3.3. - Display mode command

By pressing the orange DISPLAY MODE push-button the user gives the analyzer the order to display results already acquired, without repeating the acquisition phase. The MEAS lamp remains out.

This command allows for using all the display functions for analyzing a single recording of input data. This is useful for low or erratic repetition rate phenomena or single-shot events.

If an acquisition or clock or threshold command has been modified since the last acquisition phase, the analyzer warns the user that a command has been modified and that the results being displayed do not correspond to the next command states. The user can override this warning by pressing the DISPLAY MODE key again.

2.3.4. - Initial condition - Command state storage

At switch-on the analyzer shows successively the three command pages. The operator can use the COMMAND keys to modify commands or initiate execution of measurements.

The states of the different commands at switch-on are those that were active the last time the MEASURE or DISPLAY MODE keys were pressed before switch-off, since all command states are stored in non-volatile memories. Retention time by a non-powered instrument is 10 years. States can be read out 10^{11} times without re-writing ; 10^{6} re-write cycles are possible.

2.3.5. - 2nd file

The user has available a file in which he can store all the commands, by pressing the STORE key .

When LOAD is pressed the command states in the 2nd file are transferred into the current command file. The 2nd file is also non-volatile and is retained when power is switched off.

To avoid accidental modification of the command files (current command file and 2nd file) the user must confirm the order given to the analyzer by pressing the STORE or LOAD key twice. The order is only executed after the key has been pressed the second time.

When the 2nd file keys have been operated the analyzer displays the three command pages successively in the same way as on switch-on.

2.3.6. - Automatic offset command

This function automatically computes the offset between the trigger word and sync for analyzing, for example, a part of the displayed data with a faster time base.

1 - Execute a measurement.

2 - Place the display cursor at the start of the part to be examined with greater resolution if in record after sync mode, or at the end of the part to be expanded if in record before sync mode.

3 - Store original command states in 2nd file if required.

4 - Call up CLOCK AND THRESHOLD command page. Call up INT CLOCK PERIOD, and reduce it if in asynchronous mode.

5 - Call up ACQUISITION COMMANDS page. Call up TRI - SYNC OFFSET command and enter automatic computation mode by pressing the X key. The new value, in the range 0 to 65535, will be displayed.

6 - Execute a measurement.

7 - Return to original command configuration, if required, by pressing LOAD key of 2nd file.

This function can also be used in synchronous operation, in which case the analyzer simply records the offset set in by the display cursor position.

2.4. - COMMAND PAGE LISTS

ACQUISITION COMMANDS

0 : LOGIC	0 : negative 1 : positive
1 : FORMAT	0 : 4 chan. 1 : 8 chan. 2 : 16 chan.
2 : INPUT MODE	0 : sample 1 : latch
3 : STEPPING MODE	0 : auto 1 : ext. 2 : man. 3 : halt if different from table
4 : AUTO STEP DELAY	0 : zero 1 : 0.3 s 2 : 1 s 3 : 10 s
5 : TRIGGER QUALIFIERS	- select new value - shift cursor ← or → - valid with COMMAND
6 : TRIGGER WORD	- select new value - shift cursor ← or → - valid with COMMAND
7 : TRIGGER MODE	0 : true 1 : false
8 : TRIG - SYNC DELAY 00000 to 65535	- select new value - shift cursor ← or → X : auto compute - valid with COMMAND
9 : RECORD	0 : pre sync 1 : post sync
A : TRUTH TABLE	0 : transfer data → table 1 : transfer table → data 2 : exchange data ↔ table

CLOCK AND THRESHOLD COMMANDS

0 : CLOCK	0 : internal 1 : external + 2 : external -
1 : CLOCK QUALIFIERS	- select new value - shift cursor ← or → - valid with COMMAND
2 : INT CLOCK PERIOD	- increase with ← - decrease with → - valid with COMMAND
3 : THLD. X CHAN. Ø to 7	- select new value - sign + : 0 - : 1 - min. : - 6.35 V - max. : + 6.35 V - valid with COMMAND
4 : THLD. Y	- select new value - sign + : 0 - : 1 - min. : - 6.35 V - max. : + 6.35 V - valid with COMMAND
5 : EXT CLOCK THLD.	0 : THLD. X 1 : THLD. Y
6 : CLOCK QUAL. THLD.	0 : THLD. X 1 : THLD. Y
7 : TRIG. QUAL. THLD.	0 : THLD. X 1 : THLD. Y
8 : CHAN. 8 TO F THLD.	0 : THLD. X 1 : THLD. Y

DISPLAY COMMANDS

0 : MODE	**0 : TIMING DIAGRAM**
	1 : STATES DIAGRAM
	2 : GRAPH DIAGRAM
	3 : MAPPING DIAGRAM
1 : DISPLAYED CHANNELS	- select new value - shift cursor ← or → X : all chan. displayed - valid with COMMAND
2 : SCALE	0 : normal 1 : expand 2 : mixed

DISPLAY COMMANDS

0 : MODE	0 : TIMING DIAGRAM
	1 : STATES DIAGRAM
	2 : GRAPH DIAGRAM
	3 : MAP DIAGRAM
1 : CHANNELS 0 TO 7 BASE	0 : binary 1 : hexadecimal 2 : octal 3 : ASCII
2 : CHANNELS 8 TO F BASE	0 : binary 1 : hexadecimal 2 : octal 3 : ASCII
3 : TRUTH TABLE	0 : without 1 : with

DISPLAY COMMANDS

0 : MODE	0 : TIMING DIAGRAM
	1 : STATES DIAGRAM
	[2 : GRAPH DIAGRAM]
	3 : MAPPING DIAGRAM
1 : GRAPH SCALE	- select most signif. chan.
2 : GRAPH DOMAIN	- select new value - shift cursor ← or → - valid with COMMAND

DISPLAY COMMANDS

0 : MODE	0 : TIMING DIAGRAM
	1 : STATES DIAGRAM
	2 : GRAPH DIAGRAM
	[3 : MAPPING DIAGRAM]
1 : SCALE	0 : normal 1 : expand

3. - CIRCUIT DESCRIPTION

3. 1. - GENERAL PRINCIPLES (see block diagram)

Logic signals are buffered by three probes, transferred to the inputs and amplified and shaped.

The 16 channels of channels 0 to F are routed both to the main 4096-bit memory and to comparators which compare the input configuration bit by bit with the selected trigger word. The 4 qualifier signals are routed to an input register and to comparators. When the trigger word is detected (true triggering selected) or not detected (false triggering selected), a trigger signal is generated.

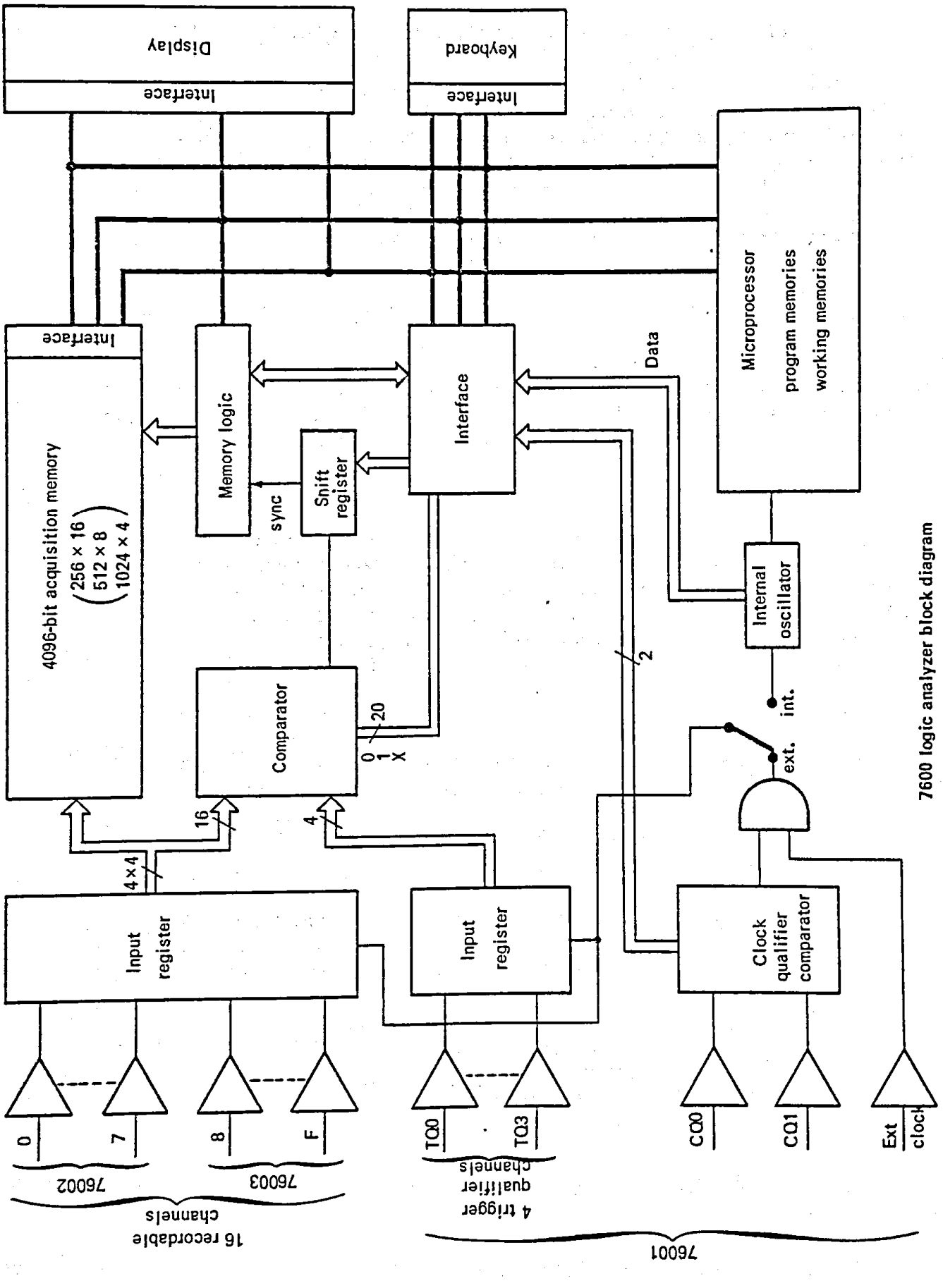
This signal is delayed by 0 to 65535 clock counts by a shift register to give the sync signal which commands recording start (record after sync) or recording stop (record before sync).

Analyzer operation is managed by a microprocessor under the control of programs stored in PROM (programmable read-only memory).

Commands are entered via a keyboard. Command states and measurement results are presented by the display unit.

Data are exchanged between keyboard, display, memory, microprocessor and the various other circuits by peripheral interface adaptors (PIAs) connected to the Address and Data buses.

Input signal sampling is controlled by an internal or external clock.



7600 logic analyzer block diagram

3.2. - INPUT PROBES (76001 - 76002 - 76003 - fig. 9 and 10)

Each probe has 8 signals applied to it and has 8 identical inputs consisting of differential amplifiers (double field-effect transistors Q1 to Q7 and Q10) which provide impedance buffering and compare the input levels with the selected logic thresholds. These thresholds, which can be different for the different sets of inputs, originate on logic board Z31.

The output from each probe input stage to the logic analyzer is via a wire pair with matching impedance of 100 Ω.

3 3. - AMPLIFIER BOARD Z1 (fig. 1)

The signals from the 76001 76002 and 76003 input probes are applied to 22 identical circuits that correspond to the 16 recordable channels, the 4 trigger qualifier channels and the 2 clock qualifier channels. The last stage includes an active clock slope selector, for the external clock input.

Description of one input stage

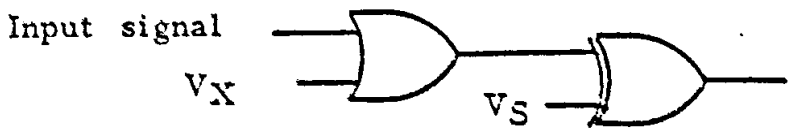
The wire pair from the probe is connected, by wires d and s, to the bases of a double transistor Qa/b configured as a differential amplifier. This amplifier shifts the common mode voltage to - 1.3 V for compatibility with the ECL circuits that follow ; the first of these is a shaper-amplifier, while the second is a trigger. The 56-Ω resistors Ra and Rb are termination loads for the twin-wire line.

Input register

Data from channels Ø to F and TVØ to TV3 are passed to flip-flops U17 - U20 - U21 - U22 - U26 for sampling at the rate set by the clock applied to their input pins 4.

Comparator

The input configuration is compared with the trigger word at the output of the input register by means of comparison of each bit with a 0, 1 or X (don't care) in OR and EXOR (exclusive OR) gates.



The truth table for the output from the comparator when a selected bit in the trigger word is compared with V_S and V_X is :

selected bit	0	1	X
V_S	0	1	1
V_X	0	0	1

The outputs from the comparators are combined in groups of 4 to give levels SY1 to SY4, which are routed to the memory buffer register (Z2 - fig. 2).

16 - 8 - 4 bit gating and shift register

The manner in which gates U43 - U44 - U45 and U46 pass input data to the shift register composed of U47 - U50 - U51 and U52 depends on word format selected.

- 16-channel format

  Data are passed directly to the register, which operates in this case as a normal latch.

- 8-channel format

  F8V is at 1 and FT4V is at 0. For each of the 4 shift-register circuits, its Q0 output is connected to its D1 input and its Q2 output to its D3 input. Channels 0 and 8, 1 and 9, 4 and 12 are grouped together and the result is a 2-bit, 2-input shift register.

- 4-channel format

  FT4V is at 1. Consecutive bits are put in series in groups of 4. U47 to U52 operate as a shift register. The input signal propagates from the Q0 outputs to the Q3 outputs at the rate set by the clock.

Trigger qualifier inputs

The signals at inputs TQØ to TQ3 are not stored in memory. Like the input signals on channels Ø to F, they are amplified and then sampled at clock rate by U26. Their comparator (an EXOR) is on the Memory board (Z2 - fig. 2).

External clock

The clock input circuit is identical to the others, but integrated circuit U11. at the output of differential amplifier Q55 - Q56, passes on either the normal signal or its complement, depending on the state of command CMFHE. Triggering therefore takes place either on the rising slope or on the falling slope of the clock.

To eliminate spurious clock pulses, the clock qualifiers are synchronized with the clock by flip-flop U25. For this to happen :

. clock qualifiers CQØ and CQ1 (after amplification and comparison, as for channels Ø to F) are applied to the D input of U25.

. U25 R input is armed by the $\overline{\text{CMHE}}$ bit from the microprocessor.

. external clock is applied to the CK input of U25, synchronizing the control signal at the inputs of gates U55.

Time base (internal clock)

This time base consists of the following elements, in order :

- a 100-MHz oscillator (integrated circuit U60 with network L1-C82-R259) which is locked to the 1-MHz signal on bus Ø2 from a crystal oscillator (Z31- fig.3)
- a divide-by-10, U62, which supplies 10-MHz signals
- gate U63 for converting this to TTL levels
- a divide-by-10, U64, which supplies 1-MHz signals
- a time base, U65, which is programmed via its 2^0 to 2^3 inputs to divide by 10^N to provide frequencies of 100 kHz, 10 kHz etc.

U68 compares the 1 MHz from U64 with the 1 MHz from bus Ø2. The resulting error voltage modulates varicap diode CR60, which controls the oscillator.

Frequencies with ratios 1. 2 and 5 are obtained by means of U61 and U57 as a function of command lines CMVHI 7, 8 and 9 :

. gate U57-14 passes on the signal directly

. U61 divides by 2 or by 5.

The clock selected by the microprocessor according to operator command is gated through first by U57-2 and -3 and then by U55. These also receive the external clock, and fan out the selected clock on 6 outputs, each of which has a matched load on every line :

. 3 outputs drive the registers and the edge detector on board Z1 ;

. 2 outputs are directly connected to the HRTE lines (input buffer register clock)

. the last output is routed to the HRTM line (memory buffer register clock) by one of the U54 gates depending on selection of 16, 8 or 4-bit word format (commanded by FT16V, FT8V and FT4V).

16-bit format : clock is passed on directly

8-bit format : clock is divided by 2 by flip-flop U56b

4-bit format : clock is divided by 4 by the two U56 flip-flops.

Glitch pulse detection

Glitch pulses on input lines between two clock pulses are detected by double type D flip-flops U15 and U16. The clock inputs of these flip-flops are both connected to the clock signal. The states of their 4 $\bar{Q}$ outputs are stored in register U27, which is enabled by bit CMDI.

When a glitch pulse occurs on an input, the logic state corresponding to this input channel is modified on the next clock edge. This change of state is commanded at the input of U47 - U50 - U51 - U52 by the logic circuit consisting of register U40 and gates U41 - U42.

Interfaces with the microprocessor

Control signals from the microprocessor are routed to the various circuits on board Z1 by three peripheral interface adapters (PIAs) connected to the data (D0 to D7) and address buses. These PIAs supply the following commands :

U70 - U71 : commands for comparing bits in the trigger word with the bits on the input channels :

V_S = signal bit
V_X = don't care

U67 : commands for enabling the internal clock (CMVHI 1 to 9), the external clock (CMHE), glitch detection (CMDI), external clock (CMFHE) and comparison signals for the CQ1 and CQ2 channels.

3.4. - MEMORY BOARD Z2 (fig. 2)

Memory buffer register and memories

The 16 signals from the shift register on Z1 are routed to the 16 random-access memories (RAMs) U5 to U7, U10 to U17, U20 to U24 via a buffer register composed of U1, U2, U3 and U4. This buffer avoids having signals that change with each clock period at the inputs of the RAMs. The 4 bits stored in one of the buffer register circuits after 4 consecutive clock periods are then passed simultaneously to the corresponding RAMs.

Each RAM has a capacity of 256 bits. Their memory locations are selected by 8 address bits, A0 to A7, from counters U55 and U56. Write into the RAMs is commanded by a 25 ns pulse on their WE inputs (pin 14).

For read-out of stored data the 16 RAMs are divided into two groups, selected one after the other by commands on their input pins 5 : one group corresponds to input channels 0 to 7, the other to channels 8 to F. Groups are selected by lines SELO7 and SELO8 from the microprocessor via PIA U45.

The RAM outputs are connected to the Data bus via inverters U25 and U26 and PIA U27.

Trigger qualification

The trigger qualifier signals, after amplification in Z1 (MS0 to MS3) are compared with the 0, 1 or X bits by gates U30 and U31. The resulting signals, together with SY1 to SY4 that result from the comparisons carried out on the channels 0 to F signals, are mixed in OR gate U32, which outputs a 0 on pin 15 if the input configuration is identical to the selected trigger word, with the complement on pin 14. These two complementary levels, which carry the trigger information are applied to 2 groups of 2 gates, U42. In each group, one or other of these gates passes on the signal depending on whether true or false triggering is selected.

One group of gates is controlled by DECO and passes the trigger signal to the memory logic if zero offset is selected.

The other group of gates passes the signal to the D inputs of flip-flops U34, if offset other than zero is selected.

Offset circuit

When the trigger word is recognized, flip-flop U34b and the shift registers are enabled.

When an offset N is selected (up to $N = 2^{16} - 1 = 65535$), the microprocessor routes the number N - 2 to the D0 to D3 Preselect inputs of counters U35, U36, U37 and U40 via PIA U44, in the form of 4 x 4 bits. Since the S1 inputs (pin 9) of these counters are at 1, they count down with each clock pulse (HRTa) on their clock inputs (pin 13). Count down is selected by a 0 on the $\overline{C}$ input (pin 10). When U35 has reached zero, it enables count down by U36 (via U41-15), etc. When all four counters have reached zero, gate U33-2 makes flip-flop U34a turn over, releasing U47a.

The counter is loaded to N - 2 since two clock pulses are used : one for triggering U34a at the start, and the other for qualifying the end of count.

Initialization

Initialization flip-flop U46a is armed through its S input (pin 5) via gates U53, U51 and U52 :

- either by PA7 from the microprocessor via PIA U45
- or by the external rate input signal enabled by PA6 from the microprocessor.

Triggering of U46a by the HRTEb clock signal in its C input enables initialization to be synchronized with the clock.

U46a is held at zero by PA4 from U45 when the microprocessor takes control of the memory logic.

The initialization signal from U46a :

- resets flip-flops U34a and b, U47a and b and U46b in the memory logic to zero
- resets the address counter U55 - U56 to zero
- sets the offset counter, via the S1 inputs, into load position.

Memory logic

The circuit is composed of a set of flip-flops :

- U47a, armed by the offset trigger (sync) signal, supplies the sync pulse when the next clock pulse arrives
- U47b, driven by address counter U55 - U56, flags when memory is filled up
- U46b, supplies the end of recording signal. It is triggered :
  - . either by U47b (AD. MAX) when memory is full, in record after trigger mode
  - . or by the sync signal from U47a in record before trigger mode.

U46b is triggered through either U52-2 or U52-3 ; these gates are controlled by the complementary outputs of U51, which itself is controlled by the microprocessor via U45 (PAØ).

The RECORDING IN PROGRESS level is routed via gate U43-15 and U45 (PB6) to the microprocessor.

This level is also passed to the enable input $\overline{E}$ of monostable U50 so that it will generate a write enable (WE) pulse for RAMs U5 to U24 with each pulse of clock HRTM. Gates U60 provide fan-out for driving all the RAM WE inputs.

The end of the WE pulse, on U50 Q output, makes address counter U55 - U56 increment.

3. 5. - LOGIC BOARD Z31 (fig. 3)

This board contains microprocessor U1 and its associated memories and interfaces

3. 5. 1. - Microprocessor

The microprocessor is a machine which, under the control of a fixed internal sequence, executes a program contained in a memory that consists of a set of operations known as instructions.

The microprocessor is thus surrounded by memories containing the programs and all information required for executing them.

The microprocessor used is a Motorola MC 6802.

Microprocessor control signals

Inputs	Functions
Extal - Xtal	Crystal connections for internal clock
Halt	Microprocessor Halt command
Reset	Interrupt used at switch-on and when re-initializing microprocessor
IRQ (Interrupt Request)	Interrupt, maskable by program
NMI	Non-maskable interrupt

Outputs	Functions
R/W (read/write)	Read or write access
VMA (valid memory address)	An address is valid
BA (bus available)	Microprocessor has halted after a Halt command
A0 to A15	16 address bits
Input/output lines	
D0 to D7	8 data bits for exchanges with outside circuitry.

Clock

The microprocessor contains a clock controlled by crystal Y1 connected between pins 38 and 39. The 1 MHz clock is made available on output pin 37 (DBE). It is inverted by U26-7 and U3-2 and then distributed on buses $\emptyset 2$ and $\overline{\emptyset 2}$.

Reset

On switch-on, after power failure, or after large power voltage variations, the change in the voltage of the + 18 V rail triggers U2, which then commands microprocessor Reset. U2 holds the Reset signal active during power up after switch-on.

Address decoding

The most significant weightings, A13, A14 and A15, are decoded by U4 which also receives the address enable signal, VMA. This circuit supplies 8 signals for selecting address groups SG0 to SG6.

3.5.2. - Memories

a) Reprogrammable read-only memories (RPROMs, type 2708)

Z31 contains 9 RPROMS (U7, U30 to U37) in which the logic analyzer operating program is stored.

Each 2708 has 1024 8-bit read-only memory locations ; their addresses are defined by the 10 bits A0 to A9.

The content of an addressed location appears on outputs D0 to D7.

Each memory is enabled on its CS/We (chip select/write enable) input by commands supplied by decoder U24 as a result of decoding bits A10, A11 and A12.

b) Random access memories (RAMs, type P2114)

There are two RAMs on Z31, U21 and U22. They store the truth table and the result of the preceding measurement. Each memory has 1024 4-bit random access memory locations.

Each memory is selected by a command on its CS (chip select) input.

The addresses are defined by 10 bits , A0 to A9, and data are inputted and outputted on the 4 lines D0 to D3/D4 to D7.

Read or write is commanded via the WE (write enable) input.

c) Electronically alterable read-only memory (EAROM)

There is a non-volatile EAROM (U20) on Z31, which stores command states. This memory is updated after each MEASURE command.

The capacity of U20 is 32 16-bit locations, addressed by 5 bits A0 to A4. Write, read and erase are commanded by 2 bits, C1 and C2 :

C1	C2	
1	1	read
1	0	read
0	1	erase
0	0	write

The memory is enabled by a 1 on its CS (chip select) input.

3.5.3. - PIAs

Like Z1 and Z2, Z31 has three peripheral interface adaptors (PIAs) type 6820 used for connecting several circuits in parallel to the microprocessor data bus.

A 6820 PIA contains 6 registers : 3 on the A side, and 3 on the B side.

The registers are addressed by signals RS0 and RS1, while the PIAs are addressed by CS0 CS1 and CS2 from the microprocessor.

PIA control

- DØ-D7 : 8 input/output lines connected to the microprocessor Data bus
- CSØ-CS1-$\overline{CS2}$: PIA selectors, connected to the addressing system
- E (enable) : PIA time reference, connected to clock Ø2
- R-S (Reset) : PIA initialization
- R/W :Read/write command from microprocessor. Connected to corresponding output from microprocessor.
- RS1-RS0 : Register select (see above)
- IRQA-IRQB : Interrupt outputs that indicate to the microprocessor that there is an interrupt from a PIA.
- PAØ to PA7 : Lines for data exchange with outside circuitry A side
- PBØ to PB7 : Lines for data exchange with outside circuitry, B side
- CA1-CB1 : Set line 7 of the control register
- CA2-CB2 : For input/output programming.

3.5.4. - Interconnections between microprocessor, memories and PIAs

Address bits A0 to A12 from the microprocessor are routed in parallel to :

- the circuit board output connector (pins 23 to 36)
- the RPROMs and RAMs via inverter buffers U5, U6 and U26.

Data bits D0 to D7 of the Program memories U30 to U37 are routed to the microprocessor by inverter buffers U25 and U26.

The Data bits, that are bi-directional information exchanged between the microprocessor and :

- PIAs U12, U16, U17
- memory U7
- RAMs U21 and U22

pass via interface buffers consisting of tri-state inverters (U10 - U11).

3.5.5. - X and Y thresholds

The logic thresholds X and Y that are allocated to the input signals are set at values between - 6.35 V and + 6.35 V in 50 mV steps.

The selected threshold values are passed by the microprocessor to PIA U17. The digital values on outputs PB and PA of U17 are converted into analog currents by converters U40 and U41 and then into voltages by operational amplifiers U42a and b.

Multiplexers U43 and U44 pass one or other of the thresholds to the input circuits of the 76001, 76002 and 76003 probes via circuit board Z1 connector.

Multiplexers U44 and U46 are controlled by PIA U16 via inverters U45 and U51. This PIA also programs the pulse width of monostable U46, which is used for inserting the wait delay in automatic rate mode.

3.6. - KEYBOARD Z5 (fig. 5)

Z5 contains :

- keys 0 to 9 and A to F of the hexadecimal keyboard : S10 to S17 and S20 to S27
- the X key (S30)
- cursor control keys S31 and S32
- control keyboard keys S1 to S7.

Data are exchanged with the microprocessor via PIA U1 which is connected to the Address and Data buses.

Control keyboard

The states of the control keys are passed to encoder U2 via debouncing circuits U7 and U10.

As soon as one key is actuated, since the R input (pin 5) of U2 is at 0, outputs 9, 7 and 6 of U2 will indicate the number of the key actuated. If two keys are actuated at once, the one with more significant weighting takes priority. In addition, U2 GS output (pin 14) goes to 0 to request an interrupt in the microprocessor.

The level supplied at the PB5 output of the PIA turns on the keyboard lamps.

Hexadecimal keyboard

These keys are interrogated by 4 columns (addressed by PIA outputs PB0 and PB1 with decoding by U3/1) and 4 rows (addressed directly by PIA outputs PA4 to PA7).

The cursor control and X keys are interrogated by PA3 together with three of the columns.

The lamps on this keyboard are controlled by shift registers U5 and U6. These are reset to zero by PIA output CA2. This makes all the lamps light. PIA output CB2 then sends as many pulses as there are lamps to turn off to the register C1 inputs. Lamps of lower weighting than the ones selected by these pulses remain turned on.

One or other of LEDs CR1 and CR2, which show whether a Command or a State is to be selected, is turned on by U3/2, which in turn is driven by PIA outputs PB3 and PB4.

LEDs CR3 and CR6, which indicate Remote Control Mode selection and Measurement in Progress, are driven by PIA outputs PB6 and PB7.

LEDs CR4 and CR5, which indicate Armed (waiting for sync) and Recording in Progress, are driven by signals originating on circuit board Z2.

3.7. - DISPLAY BOARD Z4 (fig. 4)

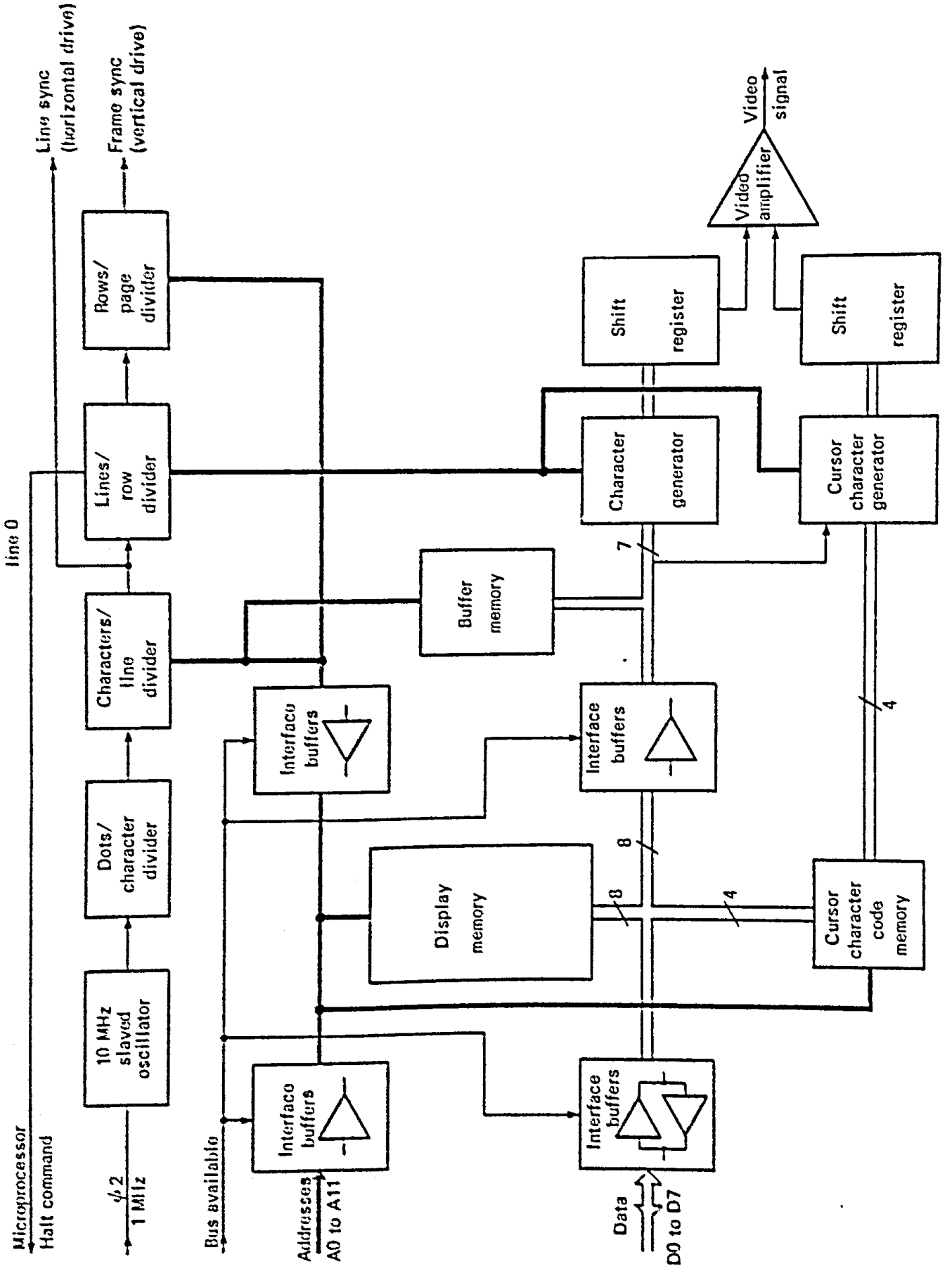
The image displayed on the screen is built up of dots. The screen is broken down into elementary squares, each consisting of 8 rows of 8 dots. Each square corresponds to one character. The 7600 can use any of 128 different characters, including 10 figures and 26 letters. The character coding is stored in a 2708 PROM (U43).

Display memory

The codes of the various characters that correspond to an image on the screen are stored in the display memory consisting of RAMs : four type P2114, U10 to U13, and 3 types 6810AP, U14 to U16.

Capacity of the display memory is 2432 (64 x 38) 8-bit words.

The microprocessor can write and read in these memory locations, with addressing by bits A0 to A11.



Block diagram of display board Z4

Buffer memory

The 64 characters in one row are placed in a buffer memory (type 6810AP) of 64 x 8 bits capacity during the first line of each row. During sweeping of the following 7 lines of this row the buffer memory provides the required data, with the result that the display memory is only occupied during one eighth of the time.

The 8 output bits from the buffer memory are passed to character generators U43 and U44 by intermediate memories U40 and U41. The first 7 bits passed to U43 define the character, while the 8th, passed to U44, indicates whether or not the cursor is on that character.

Cursor

The required form of cursor, depending on selected display mode, is stored in the memory composed of double type D flip-flop U42.

A 2708 PROM (U44) decodes the cursor character (vertical line in graphic display mode, square in mapping mode).

Shift registers

The normal channel (U43) and cursor channel (U44) character generators control two shift registers, U46 and U47 respectively ; the outputs from these registers are summed in R16 - R17 junction to drive the video amplifier.

Inverse video

Inverse video command is decoded in memory U42 and applied to the S input of RS flip-flop U45 ; the Q and $\overline{Q}$ outputs enable gates U54-8 and U54-12 respectively. In normal video , U54-8 is enabled and passes the Q output from register U46. In inverse video U54-8 is inhibited, and U54-12 passes the $\overline{Q}$ output signal from Q46.

Video amplifier

This is a conventional operational amplifier composed of transistors in U60 and Q1. At its output :

. 0 V corresponds to CRT blanking

. + 1.5 V to + 2 V corresponds to normal brightness

. + 3 V corresponds to intensification.

Synchronization

The synchronization signals are derived from a 10 MHz oscillator (U56 - U57 - U58) which is slaved to the 1 MHz microprocessor clock (bus Ø2) that originates from the crystal on board Z31 (fig. 3).

The 10 MHz signal is routed to the clock inputs of three cascaded synchronous binary dividers, U30, U31 and U32, which define :

. the dots in a character

. the characters in a line

The output from U32 is delayed by 1 clock period in U36 (see next paragraph) and then drives the clock inputs of three other cascaded dividers, U33, U34 and U35 which define :

. the lines in a row

. the rows in a page.

- The addresses defining characters in a line are routed to the display memory via interface buffers in U21, and to the buffer memory.
- Addresses defining lines in a row are routed to the character generators
- Addresses defining rows in a page are routed to the display memory via interface buffers U20.

The end of a character is detected (1 clock count early) by gate U27-8, which, by means of flip-flop U25 commands transfer of the code for the next character to character generator U43.

Detection of line Ø by gates U51-6 and U51-3 generates a $\overline{\text{HALT}}$ command to stop the microprocessor.

While the microprocessor is halted, BA is at 1, and commands :

- inhibition of buffer interfaces U1 to U4 that are between the microprocessor and the display memory, releasing the display memory for the display circuit to read out a row of characters ;
- selection of write mode of buffer memory U17 so that it can record the row of characters.

At the end of line Ø the display memory is again coupled to the microprocessor, and the buffer memory is used for displaying the next 7 lines of the row.

Propagation time compensation

The 10 MHz clock drives counters U30 to U35 which define the addresses of the dots on the screen, and also transfers data from the buffer memory to the character generator, and then from the character generator to the shift register. A delay of 1 clock pulse with respect to the dot address is accumulated with each of these transfers.

The four type D flip-flops U36 compensate for this delay of 2 clock pulses in order to supply the horizontal (line sync) and vertical (frame sync) drive signals to the CRT.

3.8. - CRT DRIVE BOARD (fig. 8)

Video amplifier

The video amplifier is Q101 (gain 15) ; its base is driven by the video signal from Z4 (fig. 4) via J101 pin 8. Q101 is turned off until the video signal becomes positive, at which moment the negative level on its collector turns the tube on directly via its cathode.

Vertical deflection

The relaxation oscillator that supplies the vertical sweep sawtooth is composed of SCR Q102 with A101 C103 and C104. These capacitors charge up exponentially until the anode voltage of Q102 becomes higher than its gate potential. Q102 then conducts and rapidly discharges the capacitors in L101. The charge rate, which defines the sweep repetition frequency, is adjusted by A101. The oscillator is synchronized by the negative signal applied to the gate of Q102, coming from Z4 via J101 pin 9.

CR101 provides temperature compensation for Q102, and facilitates its turning on and off.

Q103 acts as a reverse-biased diode to prevent the voltage going too negative. It also couples the sawtooth to output transistor Q104 via A102. Resistor bridge A102 linearizes the sawtooth by connecting Q103 emitter to the junction of C103/C104. Sawtooth slope is adjusted with A102. Its amplitude, which defines the height of the image on the screen, is adjusted by R110.

The sawtooth is applied to the vertical deflection coil L2A by Q104. Q104 is connected to the + 15 V rail by L1, the impedance of which is large compared with L2A, so that the greater part of the sawtooth current passes through L2A.

Horizontal deflection

The horizontal drive signal from Z4 (fig. 4) via J101 pin 6 is converted into a signal suitable for driving output transistor Q108 by stages Q105 and Q106, which operate as a monostable

The signal is first clipped by CR103, CR104, CR105 and differentiated by C113. Q107 discharges C112 at a rate defined by A103, when Q105 is turned off. When C112 has discharged down to 2.75 V, Q106 turns off and makes Q107 conduct. After about 25 µs, when C112 has charged up again to 8.25 V through A103, Q106 conducts, turning off Q105 and Q107, which remain turned off until the next drive pulse arrives.

C112 charging via circuit 1-3 in A103 defines the conduction time of Q107. The discharge through the centering potentiometer in A102 and Q105 sets the delay between the drive signal and the start of the sweep flyback signal.

The output stage is composed of Q108, driven by Q107 through T101 in such a way that Q108 is turned off when Q107 is turned on. At this point the energy is stored in T101. As soon as Q107 turns off, Q108 saturates. Q108 operates as a switch which is opened and closed by the signal on its base. When it conducts, C123 charges up. The deflection current increases linearly and moves the spot from the centre of the screen towards the right. Q108 then turns off. During the following negative half-cycle of the signal the spot returns to the centre of the screen. The capacitors now discharge through the deflection coil and induce a current that is the reverse of the previous one. The magnetic field developed in the coil deflects the spot towards the left.

The falling voltage across C122 makes CR111 conduct to prevent the sweep flyback pulse oscillating. The magnetic energy stored in the deflection coil is now restored to make the spot return to screen centre and to charge C123.

The cycle is repeated at the rate determined by the drive signals.

C123 blocks direct current in coil L2B and compensates for distortion at screen edges due to the curvature of the screen.

Variable inductor L103 gives adjustment of horizontal sweep amplitude.

Linearity is set by L102, as follows : during sweep flyback, C119 charges up through one winding of T2, CR112 and L102. When CR111 conducts, the deflection current in the coil falls.

The negative pulse generated during flyback is rectified by CR110 and then smoothed by C117 to provide the rail at about - 130 V which is applied to CRT grid G1 through BRIGHTNESS control potentiometer R117 (Z5 - fig. 5). This same signal is applied to transformer T2 primary. The voltages on T2 secondary are rectified by CR1, CR113 and CR114 to provide :

+ 12 kV : CRT anode bias

+ 400 V : bias for grids G2 and G4.

+ 32 V : video output stage supply rail.

3.9. - POWER SUPPLY (Z7 - Z8 - Z10, fig. 7)

The instrument is powered from 110, 127, 220 or 240 V mains. The primary circuit of transformer T1 includes a mains filter FL701, a cooling fan B701, a fuse F1, mains switch S2, and mains voltage selector S1.

The voltages from T1 secondary windings are rectified by diode bridges (CR1 to CR7, CR10 to CR17, CR20 to CR24), smoothed by capacitors C3 to C7, C10 to C12, and then passed on to the regulators to provide the - 28 V, + 18 V, $\pm$ 15 V, + 12 V, - 5.2 V, $\pm$ 5 V and - 2 V rails :

. the - 28 V rail for the EAROM (Z31 fig. 3). This is supplied by the 24 V regulator (VR1 - Z7) with adjustment by potentiometer R5.

. the + 15 V for the display unit is supplied by the + 5 V regulator (VR1 - Z8), the reference voltage of which is offset by amplifier U1 by an amount adjustable with potentiometer R7.

- the - 5.2 V rail for the ECL integrated circuits is regulated by VR3 (Z10) with adjustment by R4 to compensate for voltage drops and ensure that the rail is - 5.2 V at the board inputs.
- the + 5 V, - 2 V and - 5.2 V rails are supplied by regulators VR1 VR2 and VR3 (Z10) with extra current capacity provided by transistors Q1 to Q4.

The mechanical and electrical grounds (⏚ and ⊥) are connected together. They may be separated by cutting the jumper provided on circuit board Z7. If this is done, remove the mechanical ground wire on the CRT and wire a 0.1 µF/400 V capacitor in place of the jumper on Z7 to complete the sweep EHT circuit.

4. - MAINTENANCE

VERY HIGH VOLTAGES ARE PRESENT IN THIS INSTRUMENT WHICH CAN CAUSE INJURY OR EVEN DEATH, EXTREME CARE MUST BE TAKEN WHEN WORKING WITH THE COVERS REMOVED.

4. 1. - FRONT PANEL UPKEEP

The front panel may become dirty with use. It can be cleaned with scapy water. Do not use any sort of solvent for this operation, to avoid damaging the screen-printed legends.

4. 2. - EQUIPMENT REQUIRED FOR FAULT FINDING AND SETTING UP

Digital voltmeter

Oscilloscope (100 MHz bandwidth)

Frequency counter

Word generator

LF/HF generator (up to 30 MHz)

Generator with baseline offset facility.

4. 3. - ACCESS TO PRINTED CIRCUIT BOARDS

The four printed circuit boards Z1, Z2, Z31 and Z4 are plugged into the vertical mother board Z6. The lower circuit board , Z1, is also plugged into the front panel.

To remove one of the boards :

- unscrew and remove the board guides marked ⓑ on plate P3b.
- disconnect any wires directly connecting the board to chassis
- for the lower board, Z1, the angle bracket marked ⓐ in P3b must also be unscrewed and removed, and then all the boards plugged into the mother board pulled towards the rear. Z1 can be unplugged from the mother board Z6 once it is disconnected from the front panel.

4. 4. - FAULT FINDING

Faults in the 7600 fall into 3 general categories :

1) Power supply faults

2) Fault in one of the 2 input boards : Amplifier board Z1 or Memory board Z2 (the two lower boards ; see plate P3b). In this case the instrument will display results on the screen, but they will be incorrect.

3) Fault in one of the two logic boards : Logic board Z31 or Display board Z4 (the two upper boards). In this case the display will be incomplete, incoherent or non-existant.

The two logic boards Z31 and Z4 are serviced by the manufacturer with a board tester using the signature analysis technique. It is recommended that faulty boards of either of these two types be returned to the factory for repair.

4. 5. - TESTING AND SETTING UP

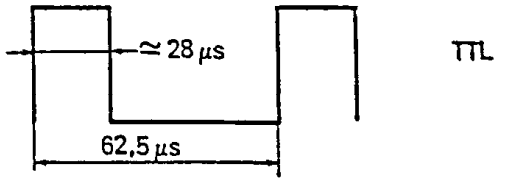
4. 5. 1. - Power supplies (fig. 7)

- Check isolation between the various power rails : - 28 V, - 15 V, - 5.2 V, - 5 V, - 2 V, + 5 V, + 12 V, + 15 V and + 18 V.
- With the mains voltage selector in the position corresponding to the local mains supply, set up :
  - . the + 15 V rail with potentiometer R7
  - . the - 5.2 V rail with potentiometer R4
  - . the - 28 V rail with potentiometer R5.
- Check the voltages of the other rails, and regulation for mains variations of ± 10%.

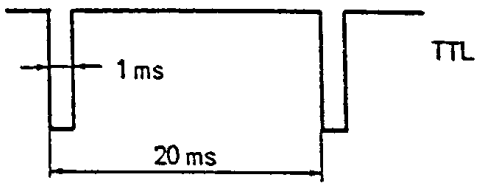
4. 5. 2. - Logic boards Z31 and Z4

- Check presence of 1 MHz clock ∅2 (duration 500 ns) on :
  - . Z31 pins 41 and 11
  - . Z4 pin 41.
- Check that oscillator U56 - U57 - U58 (Z4) is slaved to clock ∅2.
- Check for presence of sync and video on connector J101, Z4 :

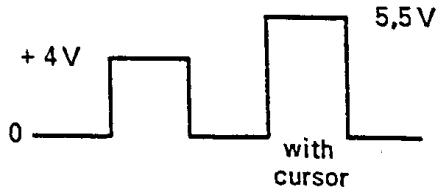
. J101 pin 6
line sync



. J101 pin 9
frame sync



. J101 pin 8
video signal



To check whether both boards Z31 and Z4 are operating correctly, call up ACQUISITION and CLOCK AND THRESHOLDS commands and verify that they operate normally.

4. 5. 3. - Sensitivity of the 23 input channels

- Using the keyboard, program thresholds of 0.00 V and adjust the X and Y ZERO potentiometers on Z31 to give 0.00 V at the threshold inputs of the probes.
- Set the logic Analyzer on : . Format : 16 channels
  . Trigger word : xxxxxxxxxxxxxxxx
  . Clock : internal (20 MHz)
  . Mode : timing diagram
- Apply on each input a 250 mV p.p, 1 MHz signal. Check on the screen, for $\emptyset$ to F channels, that the duty cycle is 1 : 1. The signal is available (TTL level) on the test points TP1 to TP7, TP10 to TP17 and TP20, on Z1. For clock, clock qual, trigger qual channels (not displayed) check the duty cycle on the corresponding test point TP21 to TP27 on Z1 (see following page).
- Reset the balance if necessary by adjusting the potentiometer in each probe input circuit. In the Ext Clock channel, adjust for best compromise between positive and negative slopes.
- Check sensitivity of each channel : . 400 mV p-p from 0 to 10 MHz
  . 800 mV p-p at 30 MHz (50 MHz typically on external clock channel).

4. 5. 4. - Internal clocks

- Connect frequency counter to test point TP30 on Z1. Program the different clock frequencies with the keyboard and check each one with the counter, pressing the MEASURE key before each measurement.
- With 10 ns clock period selected. CR60 cathode voltage should be + 4.3 V.
- Check that accuracy of 10 ns, 20 ns, 50 ns, 100 ns and 500 ms clock periods is 0.1 %.

4. 5. 5. - X and Y gains

- Select 6.35 V for X (channels 0 to 7) and Y (channels 8 to F) thresholds.
- Apply a 250 mV p-p signal superimposed on + 6.35 V dc to all probe inputs.
- Search for the channel out of 0 to 7 and 8 to F of which the value is the average of those of all the channels.
- Adjust X and Y gains with potentiometers R43 and R26 (Z31) in order to balance the two channels of amplifier U42.
- Chech that the other channels have specified accuracy ($\pm$ 50 mV $\pm$ 5%). Check in particular thresholds of - 1.3 V and + 1.5 V, that correspond to ECL and TTL levels respectively.

4.5.6. - Trigger word

- Select following parameters with keyboard :

  . Acquisition : logic : positive
  format : 16 channels
  trigger mode : true
  recording : after trigger

  . Clocks and Thresholds :
  clock : external, positive slope
  threshold : + 2 V

- Use word generator (or appropriate other circuit) to apply configurations corresponding to the outputs from a binary counter to the probe inputs. Use the counter input clock as external clock for the analyzer.

- Check that recording will start with the following words :

Ø Ø Ø Ø Ø Ø Ø Ø	Ø Ø Ø Ø Ø Ø Ø Ø
1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1
Ø 1 Ø 1 Ø 1 Ø 1	Ø 1 Ø 1 Ø 1 Ø 1
1 Ø 1 Ø 1 Ø 1 Ø	1 Ø 1 Ø 1 Ø 1 Ø

- Check true/false triggering.

- Check recording before and after sync.

4.5.7. - Trigger offset

- Display : mode : states
  code for channels 0 to F : hexadecimal

- Acquisition : trigger word for channels 0 to F :
  Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø Ø

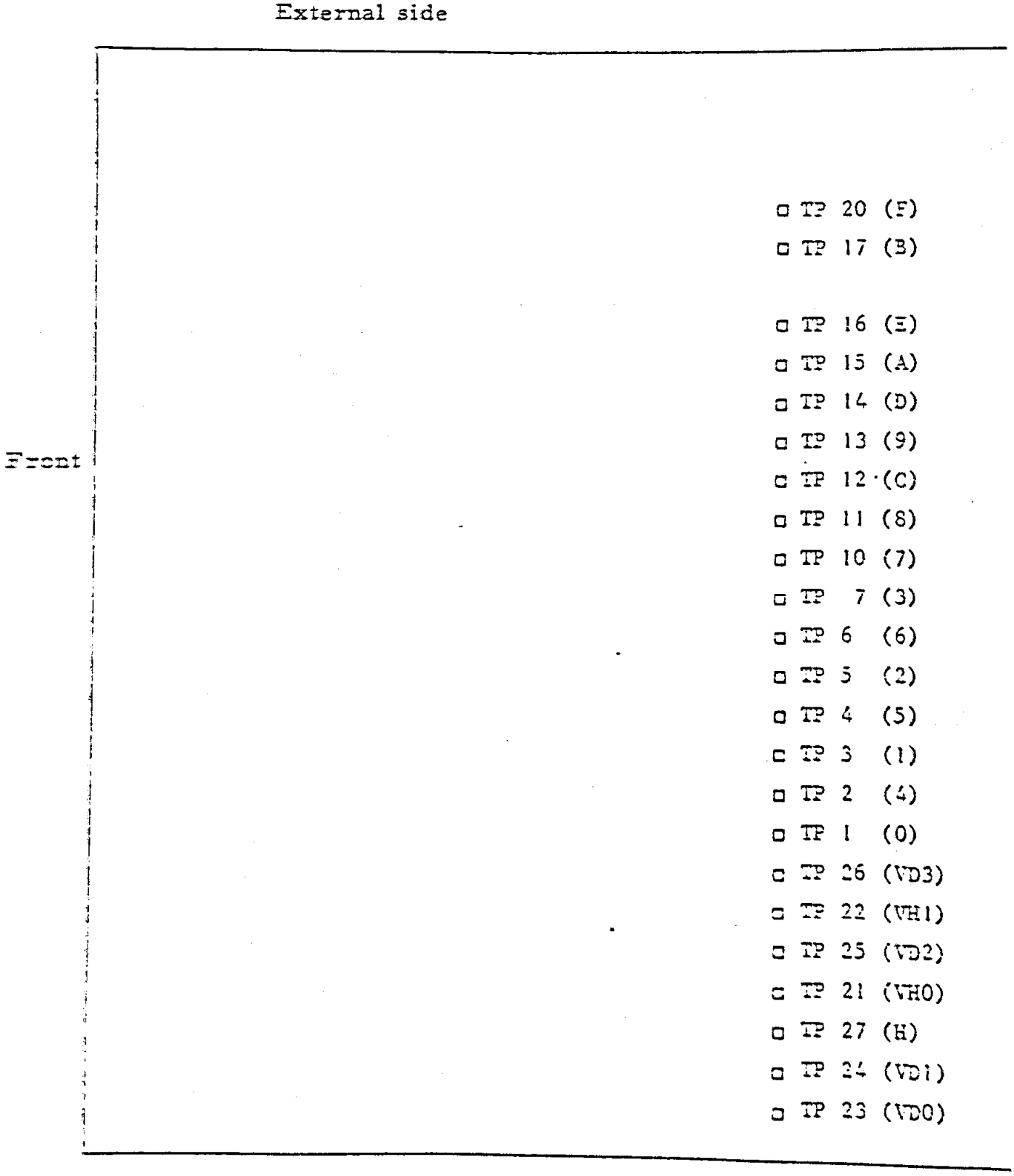
  recording : after sync.

- Clock : external

- Apply a sequence corresponding to the outputs from a binary counter to the 16 channels. Use the counter input clock as external clock.

- Check start of recording for different offset values :

Offset	start
4 3 7 1	1 1 1 3
8 7 4 Ø	2 2 2 4
1 7 4 7 8	4 4 4 6
3 4 9 5 4	8 8 8 A



Z1 - TEST POINTS SEEN ON COOPER SIDE

4.5.8. - Trigger qualifier channels

- Acquisition : format : 8 channels
  trigger word : channels 4 to F : X
- Display : mode : states
  code : binary
- Apply a 4-bit word, A B C D to inputs 0 to 3 and another 4-bit word to inputs 4 to 7 and TQ0 to TQ3.

Channel	TQ3	TQ2	TQ1	TQ0	7	6	5	4	3	2	1	0
Signal	D'	C'	B'	A'	D'	C'	B'	A'	D	C	B	A

- Check start of recording.

TQ3	TQ2	TQ1	TQ0	Recording start							
X	X	X	X	X	X	X	X	D	C	B	A
Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	D	C	B	A
1	1	1	1	1	1	1	1	D	C	B	A
Ø	1	Ø	1	Ø	1	Ø	1	D	C	B	A
1	Ø	1	Ø	1	Ø	1	Ø	D	C	B	A

4.5.9. - Measurement rate

- Check the different measurement rate modes : auto, external, manual stop if different from table.
- Check wait times with auto measurement rate :

  0 0.3 s 1 s 10 s (approx.)
- Check sync signal output on J601 (rear panel) : TTL levels.

4.5.10. - External clock qualifier channels, CQ0 and CQ1

- Acquisition : format : 4 channels
  trigger qualifiers : channels Ø and 1 : Ø
  " " " 2 to F : X
- Apply a 4-bit word (A B C D) to inputs of channels 0 to 3 and connect bits C and D in parallel to inputs CQ1 and CQ0.

- Check recording

CQ1	CQ0	Channels 3	2	1	0
D	C	D	C	B	A
Selection		Recording			
X	X	X	X	ø	ø
		or X	X	ø	1
		or X	X	1	ø
		or X	X	1	1
ø	ø	ø	ø	ø	ø
		or ø	ø	ø	1
		or ø	ø	1	ø
		or ø	ø	1	1
1	1	1	1	ø	ø
		or 1	1	ø	1
		or 1	1	1	ø
		or 1	1	1	1
ø	1	ø	1	ø	ø
		or ø	1	ø	1
		or ø	1	1	ø
		or ø	1	1	1
1	ø	1	ø	ø	ø
		or 1	ø	ø	1
		or 1	ø	1	ø
		or 1	ø	1	1

4.5.11. - Glitch detect function on channels ø to 3

Apply a pulse that is not in phase with any active clock slope to these channels and check on the screen that there is a change of state at the next clock pulse.

4.5.12. - Threshold allocation

Select the following thresholds : X : + 2.00 V
Y : - 2.00 V

- Allocate threshold X to channels 8 to F, with : trigger qualification
  ext clock
- Allocate threshold Y to the ext clock qualifier channels.
- Check that these thresholds arrive at the corresponding points of board Z9 of each probe.

4.5.13. - Truth table

Acquisition : positive logic
format : 16 channels

Display : mode : states

- Record state 0 on all 16 channels 0 to F.
- With acquisition command, transfer the data into the truth table, and then from the truth table to data.

4.5.14. - CRT drive circuit setting up (fig. 8)

The CRT, its deflection unit (fixed to the tube base socket) and the drive circuit are set up in the factory. Its adjustments should not be touched. The following may, however, be adjusted after repairs :

- vertical amplitude, with potentiometer R110
- page centering on the screen (if necessary) by moving the two correction rings on the deflection unit (the deflection unit is fixed to the CRT base socket)
- If the image is not horizontal, unscrew the deflection unit fixing screw and turn it to bring the image horizontal before locking the screw again
- Brightness level on screen : set front panel brightness control potentiometer (slider) 1 cm up from its minimum position and adjust R117 (potentiometer in parallel with brightness control) until image is just blanked
- focus : with R122
- horizontal centering of image : A103
- vertical stability : A101
- vertical linearity : A102.